Broadband Root-Mean-Square Detector in CMOS for On-Chip Measurements of Millimeter-Wave Voltages

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***Abstract*—A root-mean-square Schottky diode detector for estimating millimeter-wave (80–110 GHz) signal voltage using dc or low-frequency measurements for debugging and self-testing is demonstrated. The detector is realized in a 45-nm CMOS process without any process modifications. The detector gain at 30-mV$_{\rm rms}$ input voltage is 11 V^{-1}. The insertion loss is less than 0.2 dB, and the flatness of the detector gain over 80-110 GHz is $\pm 15\%$. The input dynamic range is greater than 29 dB, and the size of the detector including the filter capacitor is 340 μm^2.**

***Index Terms*—Detector, millimeter-wave voltage measurement, Schottky diodes.**

I. Introduction

DETECTORS for built-in self-testing that enable estimation of RF and millimeter-wave signal voltage for internal nodes of circuits using dc or low-frequency measurements have been reported [1]–[8]. However, their use has been limited primarily due to their physical size [4]–[6], [8]. The needs for the detectors are particularly great at millimeter-wave frequencies, where conventional testing is too costly. To date, one detector for millimeter-wave operation using a CMOS technology has been reported [8]. The detector was used to evaluate antenna matching at 60 GHz and occupies an area of 6400 μm^2. In addition to the size, none of the previous efforts resulted in detectors which are simultaneously compact and have high impedance (much greater than 50 Ω), wide bandwidth, and high dynamic range. In this letter, for the first time, a root-mean-square (rms) detector in CMOS that simultaneously possesses the needed properties is reported. The detector uses a Schottky diode. The measurements from 80 to 110 GHz indicate that the bandwidth is greater than 30 GHz and the insertion loss (IL) is less than 0.2 dB. The detector is fabricated in a 45-nm foundry CMOS process and requires no process modifications [9]–[11].

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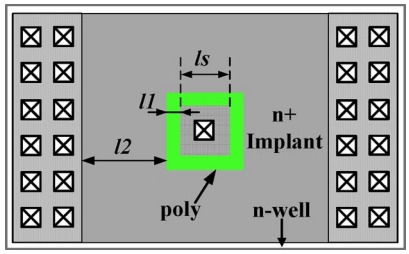

Fig. 1. Top view of polysilicon-gate-separated SBD in a 45-nm CMOS process.

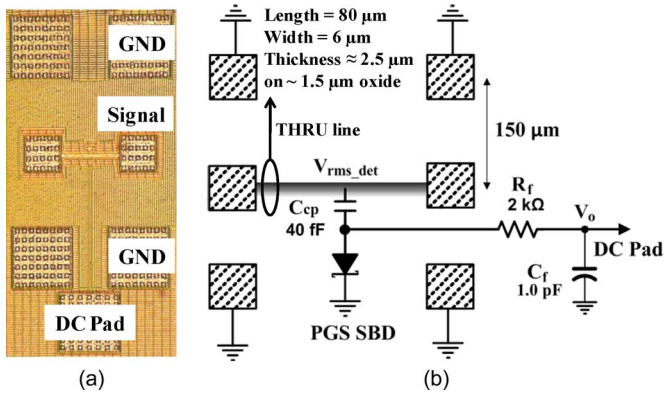

Fig. 2. (a) Die photo and (b) schematic of detector characterization structure.

II. Design

A layout of single Schottky barrier diode (SBD) cell is shown in Fig. 1. The anode of Schottky junction ($NiSi_2$) is separated from the cathodes by a polysilicon gate ring [12]. The anode area for six cells connected in parallel is 6×0.04 μm^2. The measured series resistance R_s is $\sim$10 Ω, and the zero-bias junction capacitance $C_{\rm jo}$ is $\sim$12.8 fF for a 30-cell SBD array. The cutoff frequency $[1/(2\pi R_s C_{\rm jo})]$ [13] is greater than 1 THz. The Schottky diode in addition to supporting higher frequency operation also occupies a smaller area than MOS transistor detectors at a given bias current.

The detector schematic and THRU structure are shown in Fig. 2. Starting with an 80-μm-long THRU structure (6-μm wide and $\sim$2.5-μm-thick copper layer on a $\sim$1.5-μm-thick oxide layer) and a pair of 150-μm pitch ground–signal-ground bond pads, the detector is added at the center. In addition, a dc pad is added at the bottom for biasing the Schottky diode and sensing the detected voltage. The capacitance of interdigitated metal–oxide-metal coupling capacitor ($C_{\rm cp}$) is 40 fF. The use of this small coupling capacitor is made possible by the low Schottky diode capacitance ($\sim$2.6 fF). At frequencies

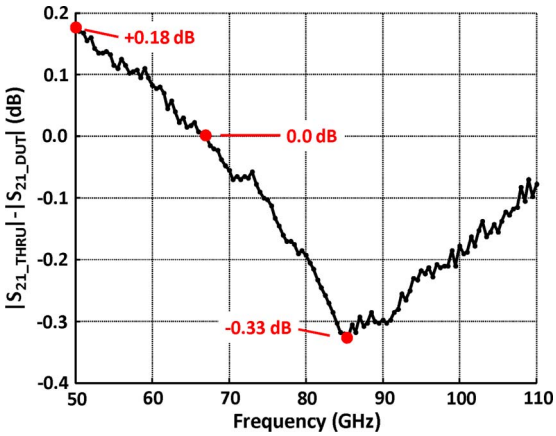

Fig. 3. IL of a six-cell SBD.

between 50 and 110 GHz, the simulated impedance looking into the Schottky diode biased with 1-μA current is mostly capacitive, and its magnitude ranges from ~850 to 410 Ω. This impedance can be made higher by reducing the number of cells. The output RC low-pass filter is composed of a 2-kΩ high-resistance polysilicon resistor (R_f) and a 1.0-pF n^+–poly-to-n-well MOS capacitor (C_f). This RC filter determines the detector bandwidth and, thus, the upper limit of modulation frequency for test signals.

III. Measurement and Results

A. Detector IL Characterization

The IL of the diode detector was estimated using the S-parameters measured with an Agilent N5250C network analyzer. Subtracting $|S_{21}|$ of THRU from that of the detector test structure (DUT), IL is estimated and plotted in Fig. 3. The IL is less than 0.2 dB between 50 and 68 GHz, and beyond 68 GHz, the loss becomes negative with the minimum of −0.33 dB. This somewhat counterintuitive insertion gain is due to the improved matching in the presence of detector. Fig. 4(a) shows that the detector exhibits better matching. $|S_{11}|$ is lower by ~0.2 dB at most frequencies above 68 GHz.

Fig. 4(b) shows the loss factor, which measures the power dissipated in the two-port network normalized by the total input power. Its expression is given in (1). The averaged data from four samples are plotted in Fig. 4, and the maximums and minimums are also plotted for both DUT and THRU. For the loss factor, the averages of differences between the maximum and minimum over the measurement frequency range for DUT and THRU are 0.022 and 0.012, respectively. The loss factor shows that the power dissipation of DUT structure is higher than that of the THRU structure in all frequencies except in the frequency range from 83 to 92 GHz. Within this range, the loss factor of THRU is slightly higher. However, the largest difference of 0.006 or 0.6% is less than the measurement tolerance. These indicate that the detector has sufficiently high impedance and can be added to circuit nodes without significantly loading down the nodes

$$\text{Loss Factor} = 1 - |S_{11}|^2 - |S_{21}|^2 \quad (1)$$

$$V^2_{\text{rms\_det}} = P_{\text{in}} \times \text{Re}(Z_{\text{in}}). \quad (2)$$

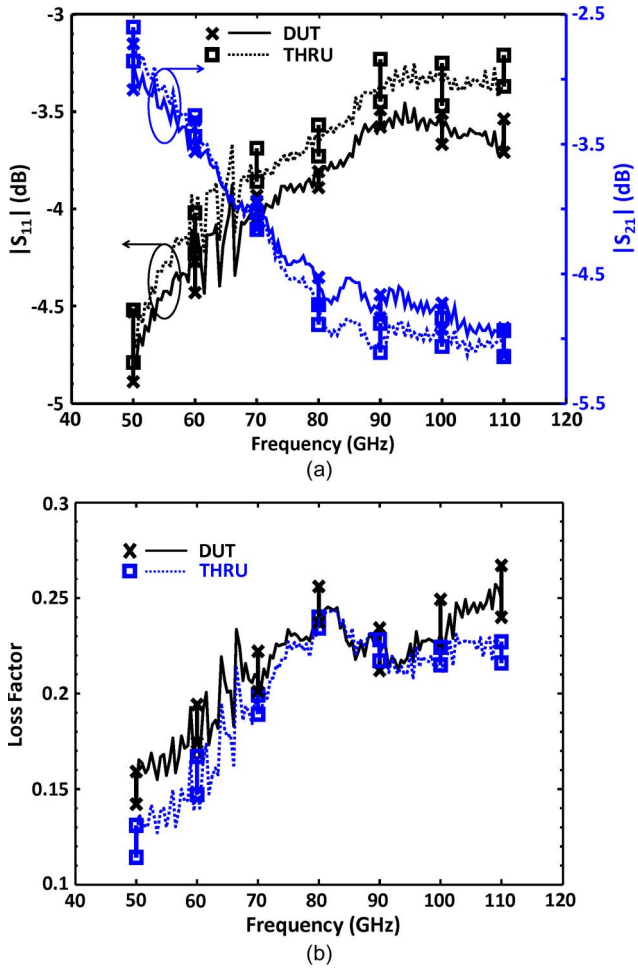

Fig. 4. (a) Input return losses $|S_{11}|$ and $|S_{21}|$ and (b) loss factor at 1-μA biased detector. Cross (×) and square (□) for DUT and THRU are the maximum and minimum measured values, respectively, for given frequency.

B. Detected Voltage and Frequency Response of Detector

The output voltage of detector at an SBD bias of 1 μA is shown in Fig. 5. The lower x-axis plots the square of RMS voltage at the detector input signal pad $V^2_{\text{rms\_det}}$, which is a function of input reflection coefficient S_{11}, or input impedance Z_{in} (at signal pad), and the power delivered to the signal pad P_{in}. $V^2_{\text{rms\_det}}$ is computed using (2). The output dc voltage V_o versus $V^2_{\text{rms\_det}}$ plots were generated at four different frequencies from 80 to 110 GHz with a 10-GHz step. The input power delivered to the port 1 signal pad is varied from −40 to −10 dBm. A dotted line with a slope of one is also shown. The output voltage V_o is measured using an Agilent Semiconductor Parametric Analyzer (E4155C), which both biases the detector and senses the detected voltage.

The input power range is bounded at the upper end by the maximum output power of an Agilent N5250C vector network analyzer which is used as an input signal source and at the lower end by the sensitivity of power sensor ELVA-1-DPM-10. The detector gain $(V_o/V^2_{\text{rms\_det}})$ is 11 V^{-1} at an input voltage amplitude of 30 $\text{mV}_{\text{rms\_det}}$. The noise floor of 1.1×10^{-4} V is calculated from measured flicker noise and calculated shot noise power spectral density at a bias of 1 μA by integrating the spectral density from 100-kHz set by the ~10-μs sampling

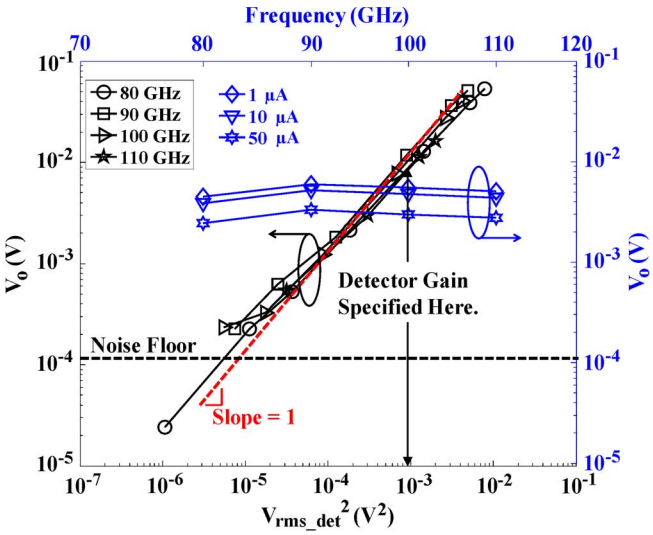

Fig. 5. (Bottom x-axis) Detected voltage versus a square of detector input voltage amplitude at four different frequencies when the diode is biased at 1 μA. (Top x-axis) Frequency response when the detector is measured at $V^2_{\mathrm{rms\_det}} = 0.002\ \mathrm{V}^2$.

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED DETECTORS

Reference	Frequency (GHz)	Area (μm^2)	Dynamic Range (dB)	Insertion Loss (dB)
[1]	0.9 ~ 2.4	31000	30	-
[4]	4.5-5.5	-	30	-
[8]	60	6400	25	-
This work	80 ~ 110[1]	340	29	less than 0.2

[1] From measured data; simulation shows 100-GHz range from 10 to 110 GHz.

time to 80-MHz set by the detector output low-pass filter bandwidth. Since the detector gain does not compress at the maximum input power for measurements, the resulting input dynamic range is greater than 29 dB. The frequency response (top x-axis) of detected voltage at detector bias current levels of 1, 10, and 50 μA is also plotted in Fig. 5. The flatness (fluctuation of V_o around the average of V_o) of frequency response between 80 and 110 GHz is less than $\pm 15\%$. The output voltage decreases with bias current, which is consistent with the detector gain expression in

$$\text{Detector Gain} = 1/\left[2 \times \mathrm{Re}(Z_{\mathrm{in}}) \times (I_D + I_S)\right]. \quad (3)$$

I_D is the dc bias current, and I_S is the diode saturation current. The frequency dependence appears to be almost independent of bias. The measured detector gains at bias currents of 1.0, 10, and 50 μA are 11.5, 9.7, and 6.3 V^{-1}, respectively. The range of gain at 80 GHz for ten measured samples measured with I_{bias} of 1 μA was $+12\%$–-11% around the mean.

IV. CONCLUSION

A compact wideband rms detector suitable for use in W-band circuits has been demonstrated in a 45-nm CMOS technology. The detector exhibits a frequency flatness of $\pm 15\%$ over 80–110 GHz and a voltage gain of 11 V^{-1} at an input voltage amplitude of 30 $\mathrm{mV}_{\mathrm{rms\_det}}$. Based on simulations, the bandwidth should be larger than 100 GHz. The low IL of less than 0.2 dB for the detector enables its use with little worry for degradation of circuit performance. Finally, the detector size including the area of C_f (110 μm^2) is 340 μm^2. More recent simulations and trial layouts indicate that it should be possible to reduce the area to less than 100 μm^2. This small size should enable wide uses in circuits. Table I compares the results of this letter to the performance of previously published detectors. The detector in this work is the only one with measured performance that is concurrently compact, sufficiently high impedance, wide bandwidth, and high dynamic range.

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