A Broadband 480-GHz Passive Frequency Doubler in 65-nm Bulk CMOS with 0.23mW Output Power

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***Abstract* — A passive 480-GHz frequency doubler based on accumulation-mode MOS varactor in CMOS process is reported. Using a compact partially-coupled ring structure, the doubler achieves a simultaneous broadband matching for fundamental and 2nd-harmonic signals. With optimized gate length and oxide thickness, the MOS varactor achieves a dynamic cutoff frequency of 870GHz while sustaining large voltage swing for high power generation. At 480-GHz output frequency, the doubler has a measured minimum conversion loss of 14.3dB and an unsaturated output power of 0.23mW. The simulated 3-dB output bandwidth is 70GHz (14.6%). The doubler is fabricated using 65-nm low power bulk CMOS technology and consumes zero DC power.**

***Index Terms* — CMOS, terahertz, frequency doubler, passive, varactor.**

I. Introduction

Terahertz frequency range (300GHz~3THz) is gaining attention for many potential applications in security, medical imaging, high-speed data transmission, and spectroscopy. In particular, signal generation near or at milli-Watt level using CMOS circuits is critical for affordable, light-weight and highly-integrated THz systems. Generally, there are two approaches to achieve this task: 1) harmonic extraction from an oscillator and 2) low-frequency source cascaded with a multiplier chain. While it is a subject of debate which method generates higher power, the former is normally more compact and power efficient; because fundamental oscillation and harmonic generation occur simultaneously. However, harmonic oscillators suffer from small frequency tuning range. The second method rectifies this problem by adopting lower fundamental frequency. The disadvantage is that since active devices are commonly used in multipliers [1]-[3], more power is consumed in multiplication stages. To exploit the latter method and overcome the power dissipation issue, a 480-GHz passive frequency doubler based on accumulation-mode MOS varactor is implemented. Using a 65-nm bulk CMOS technology (f_{max}≈210GHz), this doubler demonstrates a low-cost THz generation solution. To the best of our knowledge, this doubler provides the highest output frequency among all the CMOS frequency multipliers, and the highest power in all CMOS signal sources above 350GHz, including harmonic oscillators.

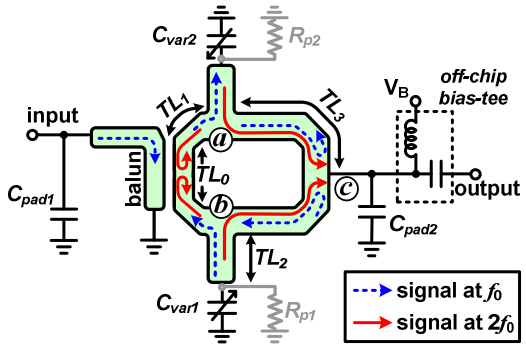


Fig. 1. Schematic of the 480-GHz varactor frequency doubler based on partially-coupled ring structure.

II. Overview of the Doubler

The schematic of the 480-GHz frequency doubler is illustrated in Fig. 1. For highest frequency conversion, we need to inject the maximum power to the varactors at the fundamental frequency (f_0) and at the same time, transfer all generated power at 2nd-harmonic ($2f_0$) to the load. This means we should simultaneously match the input to the varactors at f_0 and the output to the varactors at $2f_0$. Furthermore, we need to isolate the signal at f_0 from the output and the generated $2f_0$ from the input. Finally, since metal ohmic loss at terahertz frequencies is high, the whole doubler structure should remain as compact as possible. To achieve these conditions simultaneously, we propose a doubler based on partially-coupled ring structure.

The ring is composed of transmission line (TL) sections TL_0, TL_1 and TL_3, with symmetric branches TL_2 connecting to a pair of varactors. Since TL_0 is part of a balun and magnetically coupled to the input, signals at f_0 are differentially injected into the ring. This means when these two differential signals meet at node "*c*", they form a virtual ground which reflects the signals back so that all input power can flow into the varactors without leaking to the output. Next, the generated signals at $2f_0$ become in phase, and are combined at output node "*c*". To prevent the 2nd-harmonic signals flowing to the input port, normally a quarter-wave ($\lambda/4$) TL reflector is connected to

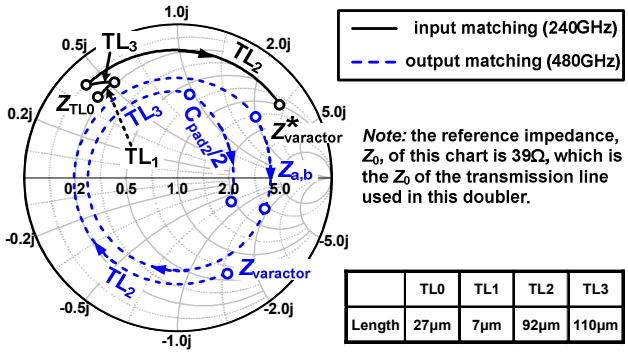


Fig. 2. Simulation of the matching scenarios of input (240GHz) and output (480GHz) using Agilent ADS and Ansoft HFSS.

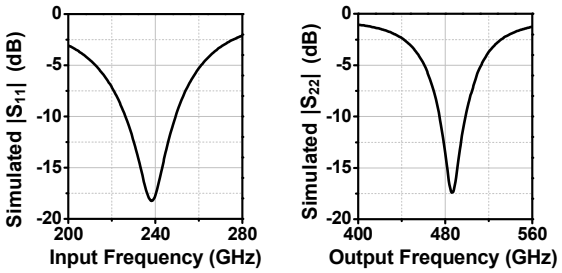


Fig. 3. Simulated large-signal input and output reflection coefficients, when the input power is 4.5dBm.

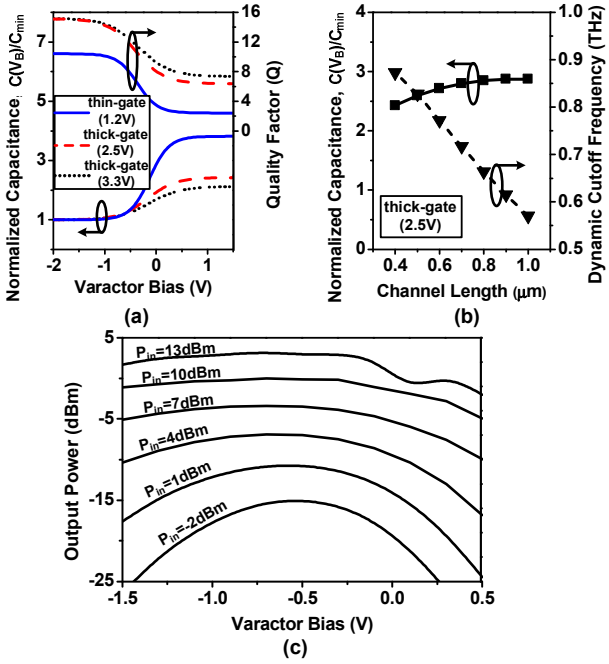


Fig. 4. Simulation results of (a) normalized capacitance and quality factor at different varactor bias, (b) normalized capacitance and dynamic cutoff frequency for different channel lengths of 2.5V thick-gate varactor, and (c) output power contour (at 480GHz) of a 2.5V thick-gate varactor at varying input power levels and bias points.

the input [2]-[4]. However, such added structure occupies large area, introduces loss to signals both at f_0 and $2f_0$, and narrows the bandwidth of the input matching network. These counteract the power recycling benefit. In the proposed ring structure, the in-phase 2nd-harmonic signals at node "*a*" and "*b*" can leak to the input port only via inter-line capacitive coupling of the balun, which can be minimized in design. Hence the conventional $\lambda/4$ TL reflector is not required.

The simulated impedance-matching scenario is shown in Fig. 2. For fundamental signal, TL_3 is close to a quarter wavelength and presents a small reactance (B_{TL3}=-$j\cdot Y_0\cdot\mathrm{ctan}\varphi_{TL3}$) at node "*a*" and "*b*", which adjusts the circle radius of the constant standing wave ratio (SWR), r_{SWR}, of Z_{TL0} so that it can then match to the varactors with a single series stub TL_2. For 2nd-harmonic signals, with series TL_2 and TL_3, $Y_{varactor}$ is transformed to an admittance with a $1/(2\cdot 50\Omega)$ real part and an inductive imaginary part. This way, matching to 50Ω output is accomplished after power combining and the resonance with the ground-shielded pad capacitance (~20fF). Fig. 3 shows that such compact ring structure achieves simultaneous broadband input and output matching.

Poly resistor R_{p1} and R_{p2} (>15kΩ) in Fig.1 are in shunt with the varactors to prevent gate oxide breakdown by accumulated charge during metal deposition. However, this increases the simulated conversion loss by 0.2dB.

III. Design Details and Simulation Results

A. Accumulation-mode MOS Varactor

For doublers based on varactors with capacitance range of C_{min}~C_{max} and series resistance of R_s, the conversion efficiency falls rapidly when the output frequency approaches the varactor dynamic cutoff frequency, ω_c, which equals to $1/(C_{min}R_s)$-$1/(C_{max}R_s)$ [5]. For the same average capacitance, thicker gate oxide results in smaller loss due to lower capacitance density, but also smaller nonlinearity C_{max}/C_{min} due to larger linear parasitic shunt capacitance. Therefore, it is necessary to optimize the varactor parameters for the highest ω_c. Fig. 4(a) shows the simulated capacitance and quality factor (Q) at varying gate bias for three gate thicknesses associated with different breakdown voltages. Varactor with 2.5-V thick gate turns out to have 10% higher dynamic cutoff frequency than the other two (870GHz versus 790GHz). Compared to thin-gate varactor, the thick-gate one also has larger power handling capability due to its higher breakdown voltage: for output power higher than -10dBm

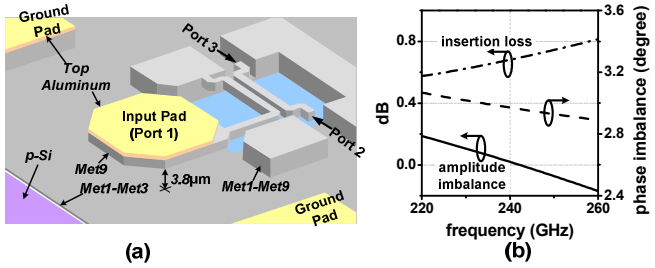


Fig. 5. A 3D illustration of the input pad and balun structure. HFSS simulated balun insertion loss, amplitude and phase imbalance are also shown.

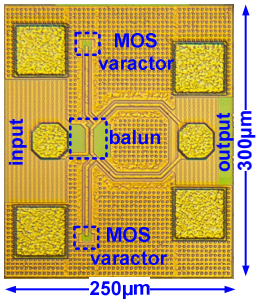


Fig. 6. Microphotograph of the 480-GHz frequency doubler.

the simulated voltage across the varactor exceeds 2V. These simulations are based on varactors with minimum gate length, because it gives the highest ω_c [6] (also simulated in Fig. 4(b)). Our doubler uses a pair of 2.5-V thick-gate varactors (W/L=(1μm×4 fingers)/0.4μm), of which the output power contour at varying input power levels and bias points is plotted in Fig. 4(c) using load-pull simulations. The predicted optimum bias point is -0.5 ~ -0.7V, and the peak efficiency is 10%.

B. Coupled-Line-Based Balun

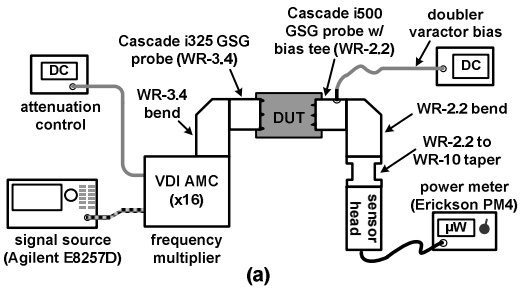
To enhance the magnetic coupling field, no ground shield is placed beneath the coupled lines. For lower eddy current induced in the lossy silicon substrate (ρ≈10Ω·cm), the metal line width should be small (3μm), so that more magnetic field is concentrated near the metal. Small line width also reduces the capacitive coupling between the two lines to isolate the 480-GHz signal from the input port, as mentioned in Section II. The HFSS-simulated insertion loss of the balun at 240GHz (shown in Fig. 5) is 0.68dB, and the output phase and amplitude imbalance across 40GHz range are less than 3.1° and 0.2dB, which enhances the broadband operation of the doubler.

C. Transmission Lines

The transmission lines of the doubler ring use GCPW structure with 3μm line width and 4μm signal-to-ground spacing. The bottom ground plane is formed by staggered-shunting M_1 to M_3 layers to comply with the maximum metal-width requirement. Due to the close proximity (3.8μm) between the signal and the ground metal, the characteristic line impedance is only 39Ω. At 240GHz, the HFSS-simulated attenuation factor of the transmission line is 1.6dB/mm.

IV. Experimental Results

The 480-GHz doubler was fabricated using 65-nm bulk CMOS technology and has an area of 300×250μm^2 (Fig. 6). Fig. 7 shows the test setup, which consists of a Cascade WR-3.4 probe fed with a VDI frequency multiplier chain as the 240-GHz input source, and a Cascade WR-2.2 probe connecting to an Erickson PM4 power meter for output power measurement. The WR-2.2 output waveguide fully cuts off the fundamental signal, and the simulated doubler's 3rd-harmonic output power is over 20dB lower than its 2nd-harmonic output. These ensure that all the power measured by the power meter is that of 2nd harmonic. Fig. 8(a) shows the measured response of the doubler versus frequency, when the input power at the probe tip is maintained at 4.5dBm using the attenuation control of the multiplier chain. Unfortunately, the frequency range provided by the input source is only 230~240GHz, which is much less than the simulated 3-dB input-referred bandwidth (35GHz) of the doubler (Fig. 8(a)). The optimum bias voltage of the doubler is -0.7V.



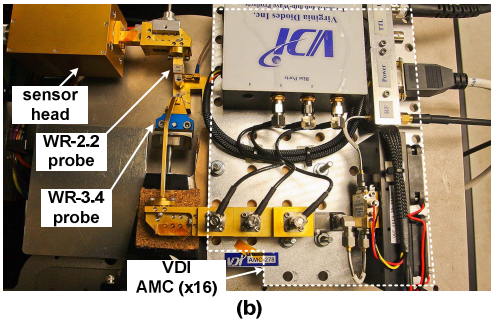


Fig. 7. Block diagram and photo of the test setup for the measurement of the 480-GHz doubler.

TABLE I
PERFORMANCE COMPARISON OF SOLID-STATE SIGNAL SOURCES

References	[1]	[2]	[3]	[4]	[7]	[8]	[9]	This Work
f_{out} (GHz)	275	325	180	125	290	482	533	480
Source Type	active doubler	active doubler	active doubler	passive doubler	harmonic oscillator	harmonic oscillator	harmonic oscillator	passive doubler
Conversion Loss (dB)	11.4	6 (gain)	6.4	10	N/A	N/A	N/A	14.3
$P_{out,max}$ (dBm)	-6.6	-3	0	-1.5	-1.2	-7.9	-36	-6.3
3-dB Output Bandwidth	7.8%	6.3%	11.1%	N/A	4.5%	0	0.1%	†14.6% (sim.)
DC Power (mW)	40	24	39	0	325	61	64	0
Technology	65-nm CMOS	130-nm SiGe	45-nm CMOS	130-nm CMOS	65-nm CMOS	65-nm CMOS	45-nm CMOS	65-nm CMOS

† Full 3-dB bandwidth could not be measured due to limited input source bandwidth (20GHz).

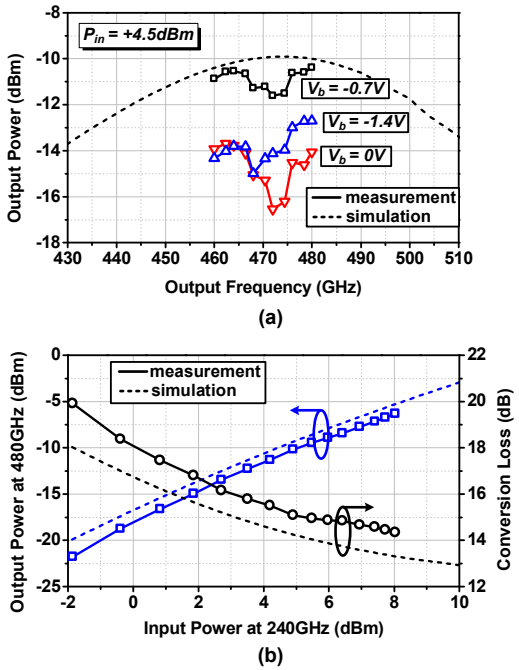


Fig. 8. Experimental results of the 480-GHz doubler: (a) output power versus the output frequency when the input power is 4.5dBm and (b) output power and conversion loss at different input power levels.

At 240GHz, the input power is swept. With the highest input available power of 8dBm, the output reaches its maximum of -6.3dBm (0.23mW). The minimum conversion loss is 14.3dB.

V. CONCLUSION

The performance comparison in Table I indicates that this doubler provides the highest frequency in CMOS multipliers and highest power among all CMOS signal sources above 350GHz. Also, apart from the protection resistors, the doubler consumes zero DC power. Since the measured output power is not saturated (Fig. 8), it is expected that the doubler is able to provide broadband half-terahertz signal with milli-Watt power level.

ACKNOWLEDGEMENT

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