25.5 A 320GHz Phase-Locked Transmitter with 3.3mW Radiated Power and 22.5dBm EIRP for Heterodyne THz Imaging Systems

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Non-ionizing terahertz imaging using solid-state integrated electronics has been gaining increasing attention over the past few years. However, there are currently several factors that deter the implementations of fully-integrated imaging systems. Due to the lack of low-noise amplification above f_{max}, the sensitivity of THz pixels on silicon cannot match that of its mm-Wave or light-wave counterparts. This, combined with the focal-plane array configuration adopted by previous sensors, requires exceedingly large power for the illumination sources. Previous works on silicon have demonstrated 1mW radiation [1,3]; but higher power, as well as energy efficiency, are needed for a practical imaging system. In addition, heterodyne imaging scheme was demonstrated to be very effective in enhancing detection sensitivity [4]. Due to the preservation of phase information, it also enables digital beam forming with a small number of receiver units. This however requires phase locking between the THz source and receiver LO with a small frequency offset (IF<1GHz). In [5], a 300GHz PLL is reported with probed output. In this paper, a 320GHz transmitter using SiGe HBTs is presented (Fig. 25.5.1). Combining 16 coherent radiators, this work achieves 3.3mW radiated power with 0.54% DC-RF efficiency, which are the highest among state-of-the-art silicon THz radiators shown in the comparison table in Fig. 25.5.6. Meanwhile, the output beam is phase-locked by a fully-integrated PLL, which enables high-performance heterodyne imaging systems.

Generally, to maximize the harmonic ($2f_0$) output power inside a radiating oscillator, it is critical to (i) achieve the optimum voltage gain of the transistor at f_0 to maximize the oscillation activity, (ii) isolate the base and collector at the harmonic to eliminate the self-power-cancelation/loading effects [1], (iii) decouple the base and collector at DC for optimum biasing, and (iv) efficiently radiate the harmonic signal without long, lossy feed lines (used for resonance at f_0 in previous works). Unfortunately, none of the previous topologies can simultaneously meet these conditions. In this paper, this is achieved in a harmonic radiator structure, which utilizes multimode wave synthesis. The radiated power and DC-to-RF efficiency are therefore fully optimized.

The radiator structure (Fig. 25.5.2) consists of two self-feeding oscillator units [1] coupled by a return-path gap (RPG). The RPG has four ports. Each two ports at top and bottom are connected in the forward current paths while separated by a metal gap in the return current paths. We will show that the RPG permits the transmission of unbalanced (differential) mode wave, while fully blocks the balanced (common) mode wave. The former case is illustrated in the left part of Fig. 25.5.3, where a pair of differential signals is injected into P_1 and P_2. The forward current on the microstrip signal trace flows into the virtual ground "*a*". Meanwhile, the differential return current, in the form of a quasi-TEM traveling wave, propagates through the central metal gap and then induces differential return (as well as forward) currents in P_3 and P_4. This means the RPG is transparent to the differential signal along P_1-to-P_3 and P_2-to-P_4 paths. To block the wave at the top/bottom boundaries of the RPG, two $\lambda_{f0}/4$ slot pairs transforming short (or virtual ground "*c*") to open are used. HFSS simulations indicate that for differential signals, the RPG has a transmission loss of only 0.6dB at f_0 (160GHz). Such broadband transparency forms the feedback paths of the two self-feeding oscillator units (Fig. 25.5.2), which provide optimum gain condition (hence maximum oscillation power) for the HBTs with proper impedance and length of the self-feeding lines [1]. Note that the RPG also separates the DC bias of the base and collector of the HBTs.

Next, for the common-mode excitation (right part of Fig. 25.5.3), the central metal gap is like a CPW without signal trace. Propagation of the symmetric wave induced by the in-phase return currents is therefore not supported. Excellent isolation between the two port pairs, shown in the simulation, is obtained. Our oscillator utilizes this behavior for three purposes: (i) at f_0, the two HBTs cannot oscillate with the undesired in-phase mode; (ii) the generated common-mode $2f_0$ signal is fully isolated between the base and collector; (iii) the slots on the top ($\lambda/4$ at f_0) now form a folded-slot antenna at $2f_0$, which instantly radiates the harmonic signal to the chip backside without feed lines. This greatly reduces the signal loss and chip area. The simulated radiation pattern of each radiator is shown in Fig. 25.5.3. The estimated radiation efficiency (including the reflection at silicon-to-air interface) is ~50%. It is also noteworthy that the $2f_0$ signal is generated by the nonlinear heterojunction at the base of the HBT. Such technique recycles the fundamental oscillation power dissipated at the base, and efficiently upconverts it to $2f_0$. From the above analysis, it can be seen that through the synthesis and guidance of different electromagnetic wave modes, we have optimized the fundamental oscillation, harmonic generation and radiation with a very compact passive structure.

In the transmitter, 16 radiators combine their power in free space. For coherency, they are injection-locked by 4 mutual-coupled VCOs (Fig. 25.5.1). Based on differential Colpitts topology, the VCOs oscillate at 80GHz with second-harmonic extraction to drive 4 160GHz buffers. One VCO also connects to a divider chain inside a PLL. It is noteworthy that the PLL has a controllable fractional-N capability. When the transmitter pairs with a heterodyne receiver, where an identical PLL (with fractional-N disabled) is built-in to generate LO, desired RF-to-LO frequency offset (~100MHz) is obtained. In such imaging system, only one low-frequency reference clock (~312MHz) is needed.

The transmitter is implemented using a 0.13μm SiGe:C BiCMOS process (f_T/f_{max}=220GHz/280GHz [6]). The measurement setup is shown in Fig. 25.5.4, where the radiation spectra are measured by a WR-3 horn antenna cascaded with a VDI Even-Harmonic Mixer (EHM). It can be seen that the radiators are synchronized by the on-chip PLL. The measured output frequency is 317GHz. To eliminate the substrate wave caused by the silicon substrate, a hemispheric (radius=5mm), high-resistivity Si lens is attached on the chip backside. The measured radiation patterns with and without the lens are shown in Fig. 25.5.5, which have a directivity of 17.3dBi and 13.0dBi, respectively. The difference is due to the refraction at the silicon-to-air interface (without lens). Using an Erickson PM4 calorimeter, the radiated power/EIRP (with silicon lens) are measured at varying distances and radiator DC supplies. Shown in Fig. 25.5.5, the measurement is consistent with the Friis equation in far-field range above 5cm. The peak EIRP and total radiated power are 22.5dBm and 5.2dBm (3.3mW). Without the silicon lens, the EIRP is 13.9dBm, and the radiated power only drops to 0.9dBm (1.23mW), which is still higher than [1,2,7] and [8]. Finally, the micrograph of the die and a performance comparison with the state-of-the-art are given in Fig. 25.5.6. This work demonstrates fully-integrated phase-locking capability, and the highest output power and DC-to-RF efficiency among the silicon THz radiators listed in the Table.

Acknowledgements:
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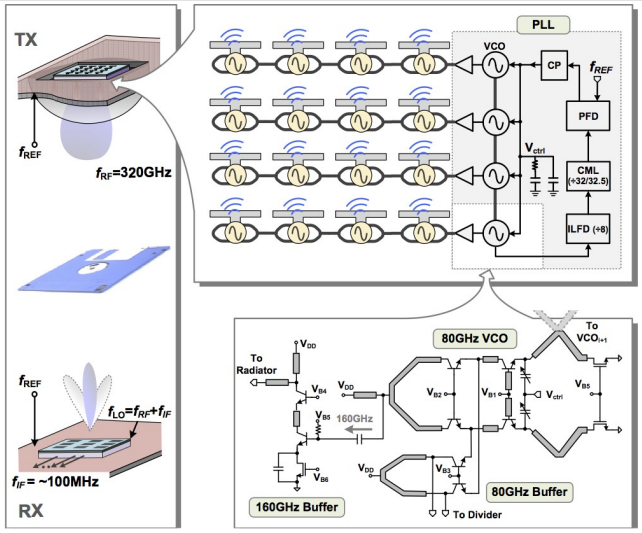


Figure 25.5.1: Architecture of the 320GHz transmitter for heterodyne imaging systems.

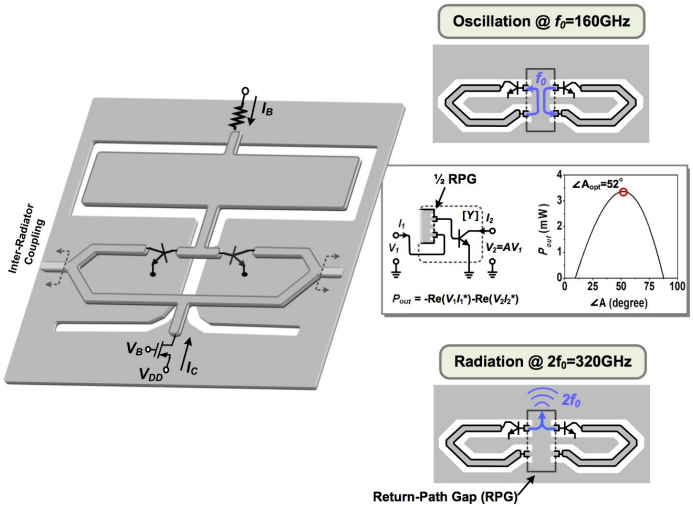


Figure 25.5.2: Return-path gap radiator and its operations at f_0 (as two self-feeding oscillators) and $2f_0$ (as a harmonic radiator). The simulated optimum phase of the transistor (plus half RPG) at f_0 is also shown.

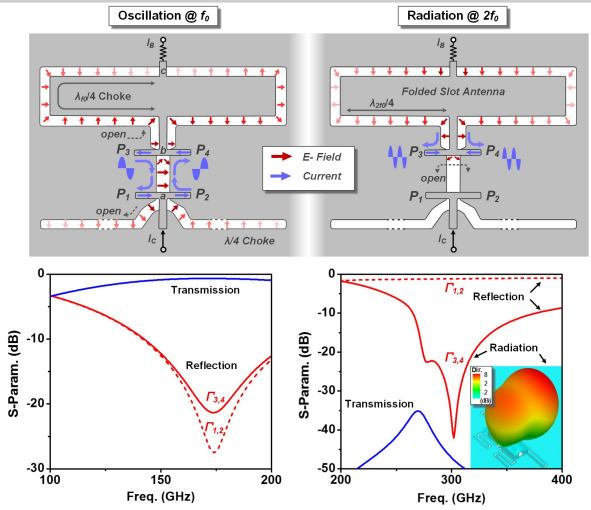


Figure 25.5.3: The EM field distribution and simulated insertion loss of the RPG structure for (left) differential oscillation at f_0 and (right) common-mode harmonic generation/radiation at $2f_0$.

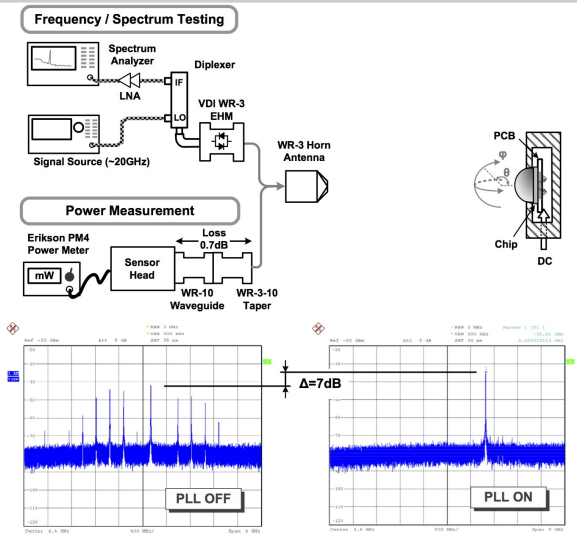


Figure 25.5.4: Measurement setup and the measured spectra of the downconverted radiation (with and without radiator synchronization).

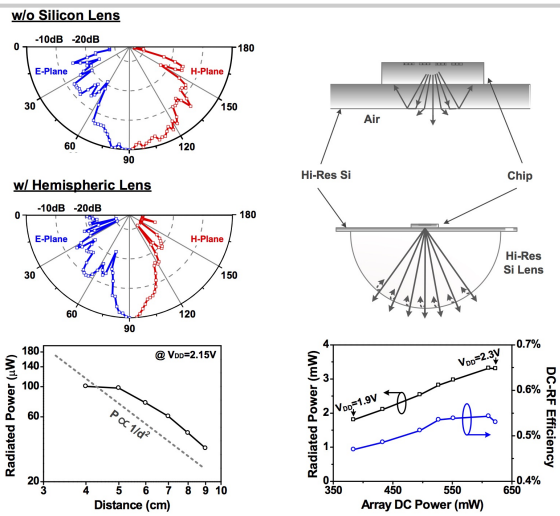
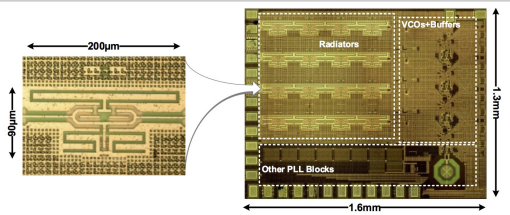


Figure 25.5.5: (Top) Measured radiation pattern, (bottom left) received radiation power versus distance, and (bottom right) total radiated power and DC-to-RF efficiencies at different power supplies.



	Technology (f_{max})	Freq. (GHz)	Radiated Power (dBm)	EIRP (dBm)	Phase Noise (dBc/Hz[1/2])	DC Power (W)	Radiator Efficiency (%)	Integrated Phase Locking?
ISSCC 2013 [1]	65nm CMOS (250GHz)	260	0.5 †	15.7	-78.3 @1MHz	0.8	1.4	No
ISSCC 2014 [2]	130nm SiGe (500GHz)	530	0 †,††	25	N/A	2.5	0.4	
IMS 2013 [3]	130nm SiGe (500GHz)	245	1 †††	7	N/A	0.38	3.3	
ISSCC 2012 [7]	45nm CMOS (190GHz)	280	-7.2 †††	9.4	N/A	0.82	0.23	
ISSCC 2014 [8]	65nm CMOS (250GHz)	338	-0.9	17.1	-93 @1MHz	1.54	0.53	
JSSC 2013††††	65nm CMOS (190GHz)	288	-4.1 †	N/A	-87 @1MHz	0.28	1.4	
This Work	130nm SiGe (280GHz)	317	0.9	13.9	-79 @1MHz	0.61	2.0	Yes
			5.2 †	22.5			5.4	

†: Silicon lens is used
††: Radiation is not coherent
†††: Substrate thinning is used
††††: J. Grzyb, et al, IEEE JSSC, vol. 48, no. 7, 2013

Figure 25.5.6: Chip micrograph and performance comparison with other state-of-the-art silicon-based radiators in sub-THz/THz range.

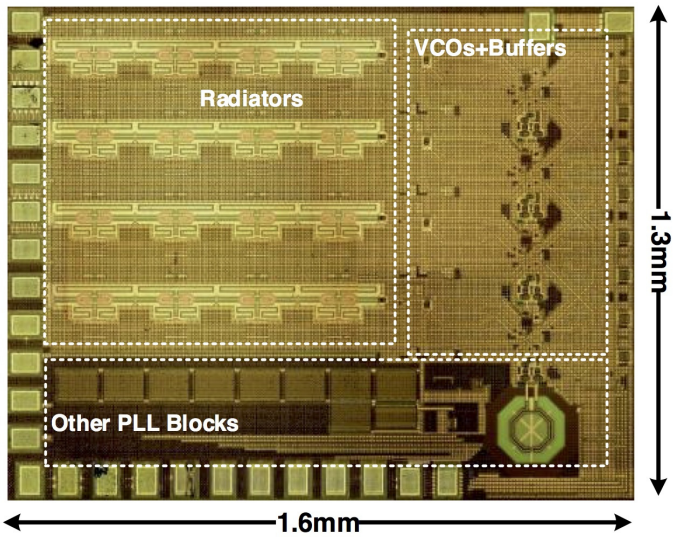


Figure 25.5.7: Die micrograph of the 320GHz SiGe Transmitter.