

A Fully Integrated 320 GHz Coherent Imaging Transceiver in 130 nm SiGe BiCMOS

Chen Jiang, *Student Member, IEEE*, Ali Mostajeran, *Student Member, IEEE*, Ruonan Han, *Member, IEEE*,
 Mohammad Emadi, Hani Sherry, *Member, IEEE*, Andreia Cathelin, *Senior Member, IEEE*,
 and Ehsan Afshari, *Senior Member, IEEE*

Abstract—A 320 GHz fully integrated terahertz imaging system is reported. The system is composed of a phase-locked high-power transmitter and a coherent high-sensitivity subharmonic-mixing receiver, which are fabricated using a 130 nm SiGe BiCMOS technology ($f_T/f_{\max} = 220/280$ GHz). To enhance the imaging sensitivity, a heterodyne coherent detection scheme is utilized. To obtain frequency coherency, fully integrated phase-locked loops are implemented on both the transmitter and receiver chips. According to the measurement results, consuming a total dc power of 605 mW, the transmitter chip achieves a peak radiated power of 2 mW and a peak EIRP of 21.1 dBm. The receiver chip achieves an equivalent incoherent responsivity of more than 7.26 MV/W and a sensitivity of 70.1 pW under an integration bandwidth of 1 kHz, with a total dc power consumption of 117 mW. The achieved sensitivity with this proposed coherent imaging transceiver is around ten times better compared with other state-of-the-art incoherent imagers. To the best of our knowledge, this paper demonstrates the first fully integrated coherent terahertz imaging transceiver on silicon.

Index Terms—BiCMOS, coherent imager, heterodyne detection, phase-locked loop (PLL), return-path gap coupler (RPGC), sensitivity, SiGe, subharmonic mixing, terahertz imaging, transceiver.

I. INTRODUCTION

DUE to the emerging applications in security screening [1], biology [2], medical diagnosis [3], and material characterization [4], terahertz imagers are attracting increasing attention. Compared with microwave frequencies, the shorter wavelength could effectively enhance the spatial resolution. Compared with X-ray, the nonionizing nature makes it more preferable in many applications. As the development of fabrication and design techniques, silicon platform is becoming more and more attractive and suitable for terahertz imagers implementation, since it could provide much higher integration level and yield, as a result, significantly lower cost and smaller size.

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C. Jiang, A. Mostajeran, and E. Afshari are with the Department of Electrical and Computer Engineering, Cornell University, Ithaca, NY 14853, USA, and the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109, USA (cj342@cornell.edu).

R. Han is with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

M. Emadi is with Qualcomm Inc., San Jose, CA 95110 USA.

H. Sherry and A. Cathelin are with STMicroelectronics, 38920 Crolles, France.

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According to Planck's law of thermal radiation, terahertz wave is emitted from any warm body as part of the blackbody radiation [5], but the emitted power is normally very weak. Due to the limited sensitivity of current silicon detectors, the active imaging scheme is more practical, which means that a high-power terahertz radiating source is needed for illumination. As a result, a lot of research effort was made on silicon terahertz source design and significant progress has been made. In [6], a 280 GHz 4×4 radiating array capable of beamsteering is presented, which achieves a 0.19 mW output power and a 9.4 dBm EIRP. A 338 GHz 2-D 4×4 phased array is introduced in [7], and the obtained output power and EIRP are 0.81 mW and 17.1 dBm, respectively. In [8], a 530 GHz source module with up to 1 mW output power for diffuse illumination is demonstrated. To form a complete imaging system, a terahertz detector is needed to pair up with the source. Previous works have also demonstrated terahertz detectors on silicon successfully. Using Schottky barrier diodes, a 280 GHz 4×4 array and an 860 GHz detector cell are demonstrated, achieving minimum NEPs of 29 and 42 pW/ $\sqrt{\text{Hz}}$, respectively [9]. In [10], a 320 GHz 4×4 imaging array in a SiGe technology is presented, which is measured to have an average NEP of 34 pW/ $\sqrt{\text{Hz}}$. In [11], a 1 kpixel terahertz imaging camera chip at 860 GHz is introduced, which achieves an NEP of 100 pW/ $\sqrt{\text{Hz}}$.

However, since most of the previous works are based on incoherent direct detection, the sensitivity is limited. Consequently, in order to obtain a reasonable dynamic range, normally an off-chip high-power source is needed for illumination [9]–[11]. In order to implement a fully integrated terahertz imager, the detector sensitivity needs to be improved to alleviate the output power requirement on the source, so that an on-chip source would suffice. To enhance the detector sensitivity, the heterodyne detection scheme can be used [12]. However, this requires frequency coherency between the source and the detector. To achieve this, multiplier-chain-based sources could be used, but they are normally less power efficient and need RF input sources [13]. Fortunately, the phase-locked terahertz sources on silicon have been demonstrated recently. In [14], a 300 GHz phase-locked loop (PLL) is introduced, which can provide a 40 μW probed output power. In [15], a 320 GHz transmitter chip with on-chip PLL achieving a 3.3 mW output power and a 22.5 dBm EIRP is demonstrated.

In this paper, a 320 GHz coherent imaging transceiver is presented. In the transmitter chip, a 4×4 radiator array is injection locked to an on-chip PLL to provide terahertz illumination.

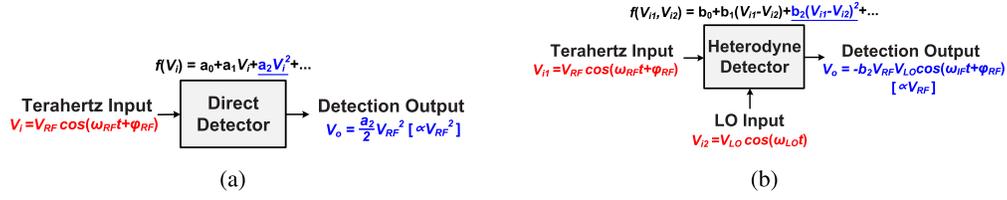


Fig. 1. Principles of (a) incoherent direct detection and (b) coherent heterodyne detection.

In the receiver chip, an eight-cell subharmonic-mixing detector array is used to perform a coherent heterodyne detection to enhance sensitivity. Fabricated with a 130 nm SiGe:C BiCMOS process, the transmitter achieves a 2 mW output power and a 21.1 dBm EIRP. The receiver achieves a 31 V/V RF-to-baseband voltage conversion gain. With a 1 kHz bandwidth (corresponding to a 1 ms time constant for fast imaging), the proposed coherent imager achieves a sensitivity of 70.1 pW. Compared with other state-of-the-art incoherent imagers, it is around ten times better. The sensitivity enhances even further with larger bandwidth (around 20 times for 10 kHz and around 70 times for 100 kHz) corresponding to faster imaging. Even though coherent imaging has been demonstrated previously, all of them use multiplier-chain-based sources [16] or injection lock on-chip sources to outside signal [17], which all require high-frequency high-power RF inputs. Using the PLL-based structure, this paper demonstrates the first fully integrated coherent terahertz imaging transceiver on silicon.

In Section II, principles of the coherent heterodyne detection and the transceiver architecture are introduced. The transmitter architecture and detailed circuit blocks design are given in Section III. The subharmonic-mixing receiver design is presented in Section IV. The experimental results of the imager prototype are presented in Section V. Finally, a performance summary and comparison with some state-of-the-art imagers as well as a brief conclusion are given in Section VI.

II. PRINCIPLES OF HETERODYNE DETECTION AND SYSTEM ARCHITECTURE

Due to the limited f_{\max} and breakdown voltage of silicon transistors, obtaining high output power is still challenging. With the current silicon sources, in order to achieve high dynamic range for high-quality imaging, the sensitivity of the detector needs to be enhanced.

A. Heterodyne Detection and Direct Detection

The conventional incoherent direct detection scheme is shown in Fig. 1(a). If an input signal $V_{RF} \cos(\omega_{RF}t + \phi_{RF})$ is applied, the produced dc output change will be $a_2 V_{RF}^2/2$, where a_2 is determined by the nonlinear device used. Due to its simplicity, this scheme is used in most of the previous works [9]–[11], [18]. To alleviate the impact of the device flicker noise, the output signal is normally chopped to an IF frequency. As a result, the output IF signal (fundamental

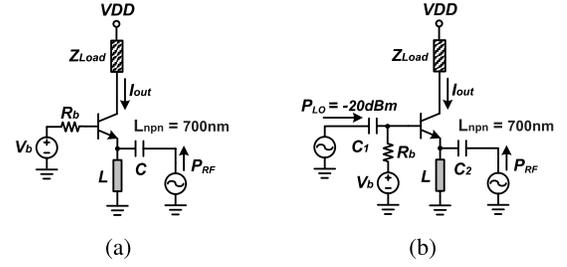


Fig. 2. ST 130 nm BiCMOS bipolar transistor with a 700 nm emitter length configured as a (a) direct detector and a (b) heterodyne detector.

tone of the square wave after chopping) is

$$V_{IF}(t) = \frac{1}{\pi} a_2 V_{RF}^2 \cos(\omega_{IF}t) \quad (1)$$

in which ω_{IF} is the chopping frequency. In the heterodyne detection scheme, the input terahertz signal is mixed with a local oscillation (LO) signal to generate the output IF signal, as shown in Fig. 1(b). In this case, if a terahertz input of $V_{RF} \cos(\omega_{RF}t + \phi_{RF})$ and an LO of $V_{LO} \cos(\omega_{LO}t)$ are applied, the output IF signal can be written as

$$V_{IF}(t) = -b_2 V_{RF} V_{LO} \cos(\omega_{IF}t + \phi_{RF}) \quad (2)$$

in which ω_{IF} equals the frequency difference between the RF and LO, ϕ_{RF} represents the phase of the RF signal, and b_2 is the mixing coefficient of the device. Comparing (1) and (2), we can see that in the heterodyne detection case, the followings hold.

- 1) The output drops with V_{RF} instead of V_{RF}^2 , meaning when the RF signal is weak, the output of a heterodyne detector drops much slower compared with that of a direct detection one.
- 2) The output signal is also proportional to V_{LO} . Normally, as the LO power is considerably higher than the RF signal, the output signal will also be stronger.
- 3) Phase information of the RF signal (ϕ_{RF}) is preserved at the output. As a result, electrical scanning based on digital beamforming is achievable, which has the potential to replace the traditional mechanical scanning to significantly reduce the imaging time.

Therefore, the heterodyne detection scheme can largely enhance the detector performance. For a further comparison, a bipolar transistor is configured both as a direct detector [input power injected from the emitter, as shown in Fig. 2(a)] and a heterodyne detector [input power injected from the emitter and -20 dBm LO power pumped into the base,

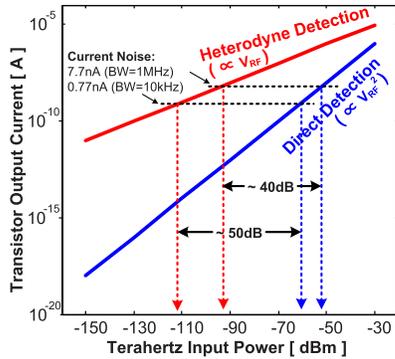


Fig. 3. Comparison simulation results using the ST 130 nm BiCMOS bipolar transistor.

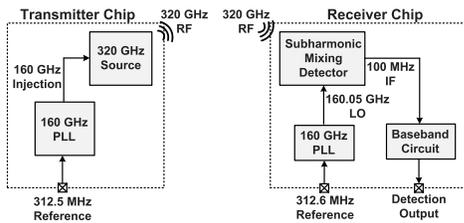


Fig. 4. PLL-based subharmonic-mixing heterodyne detection transceiver architecture.

as shown in Fig. 2(b)]. The simulated output current with different RF powers in both cases is shown in Fig. 3. It is obvious that under low RF power, which is the real scenario in most applications, the heterodyne detection scheme shows a great advantage. With an assumed bandwidth of 1 MHz, the simulated integrated current noise is 7.7 nA. Under this circumstance, to achieve a signal-to-noise ratio (SNR) of 1, the required input power of the heterodyne detector is around 40 dB lower than that of the direct detector. If a bandwidth of 10 kHz is chosen, the difference becomes 50 dB, as shown in Fig. 3.

B. Subharmonic-Mixing Heterodyne Transceiver Architecture

The heterodyne detection scheme requires frequency coherency between the transmitter and the receiver in order to obtain an output signal with a stable frequency. Frequency coherency can be obtained using multiplier chains; however, it has two obvious drawbacks: 1) it needs high-power high-frequency sources and 2) the dc-to-RF efficiency is normally low compared with oscillator-based sources [13]. In order to achieve higher integration level and better power efficiency, a PLL-based transceiver architecture shown in Fig. 4 is proposed. In the transmitter, the 320 GHz radiator is injection locked to a 160 GHz PLL. There is one important issue that needs to be addressed: the radiator is required to generate high output power, which needs the oscillators in the radiator to have a large oscillation activity. However, the power injected into the radiator is limited due to the power consumption restriction of the PLL. As a result, the radiator can only be locked within a limited range near its free-running frequency [19]. Fortunately, the heterodyne detection scheme

does not require large frequency tuning. However, since the free-running frequency of the radiator is hard to predict accurately due to the inaccurate device model at high frequency and process variation, the PLL needs to have a sufficient tuning range to cover the possible frequency shift of the radiator. In the receiver, the phase-locked 320 GHz RF signal is mixed with the 160.05 GHz LO generated by the receiver PLL. Ideally, we could use the PLL to injection lock another 320 GHz oscillator to generate the LO signal. However, with a large oscillation activity in the 320 GHz oscillator, the tuning range for the LO is largely reduced as discussed before. Due to the possible frequency mismatch caused by process variation between the transmitter and receiver, such a small locking range may not be able to ensure frequency coherency. To address this issue, even with a relatively larger conversion loss, the subharmonic-mixing scheme is still used to obtain a wider LO tuning range to ensure frequency coherency. Moreover, in this scheme, the PLL in the transmitter can be reused in the receiver with minor modifications, which makes it much simpler and also causes less frequency mismatch. After the subharmonic mixing, the output 100 MHz IF signal is then processed by the on-chip baseband circuits. The detection output is finally collected and sent to a computer for image construction.

III. DESIGN OF THE HIGH-POWER PHASE-LOCKED TRANSMITTER

Even though the heterodyne detection scheme could enhance the sensitivity of the detector, it is still desirable to achieve high output power for better image quality. Shown in Fig. 5 is the architecture of the high-power 320 GHz phase-locked transmitter. Sixteen radiator cells form a 4×4 radiator array with their power adding up in free space. The radiator array is then injection locked by the 160 GHz PLL. A similar architecture is reported in [15]; however, only a 200 MHz tuning range is achieved at the 320 GHz output. It will be shown later that patch antennas are used on the receiver side, which have a narrow bandwidth. In order to ensure that the transmitted frequency falls inside the receiver antenna bandwidth, a much larger frequency tuning range is desired. Next, design details of some critical circuit blocks are given.

A. Radiator Array

Since the targeted frequency is higher than the f_{\max} of the transistors in this 130 nm BiCMOS process ($f_{\max} = 280$ GHz [20]), harmonic oscillators are used. It has been shown in [15] that there are several conditions for maximizing the radiated harmonic power.

- 1) Shown in Fig. 6 is a two-port network representation of a bipolar transistor. As shown in [21], there is an optimum phase condition for the complex voltage gain A to maximize the fundamental oscillation activity: $\angle A_{\text{opt}} = \angle - (y_{21} + y_{12}^*)$.
- 2) Isolation between the base and collector of the transistor at the desired harmonic frequency is necessary to eliminate the self-power-cancellation/loading effect [21].

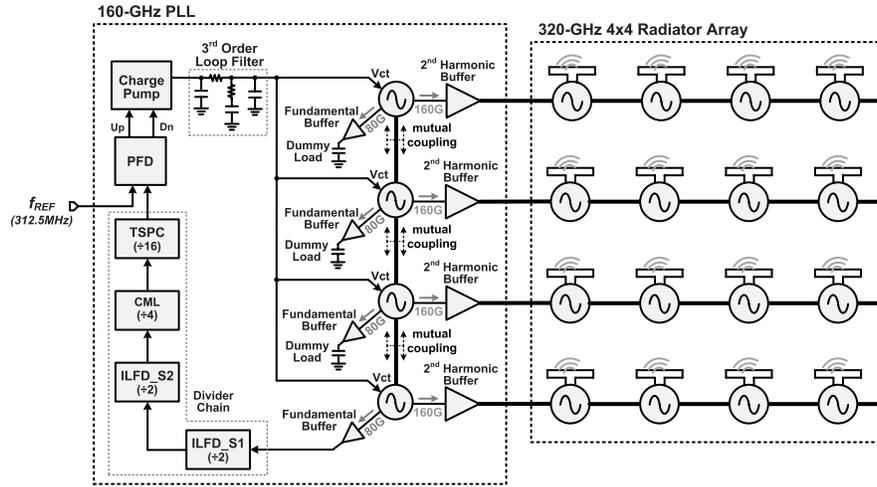


Fig. 5. High output power 320 GHz phase-locked transmitter architecture.

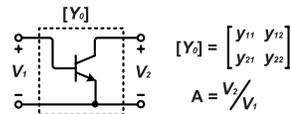


Fig. 6. Two-port network representation of an n-p-n transistor.

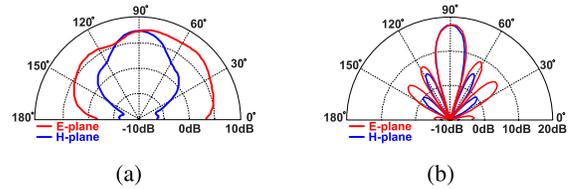


Fig. 8. Simulated radiation pattern of (a) one radiator cell and (b) 4 × 4 array.

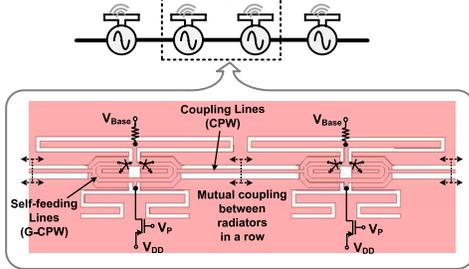


Fig. 7. Radiator cells and coupling between them.

- 3) Efficient harmonic signal radiation near the transistor is desired in order to avoid additional feed line or matching network loss.

In [15], a return-path gap coupler (RPGC) based self-feeding oscillator structure is presented, which can simultaneously meet all the aforementioned conditions. Utilizing this structure, two adjacent radiator cells are shown in Fig. 7. The self-feeding lines are used to achieve the optimum phase condition for the transistors. Since the RPGC is opaque to even-mode signals, isolation between the base and collector at second harmonic is achieved [15]. Besides, the generated harmonic power is instantly radiated by the top slots without experiencing additional loss caused by the feed lines and matching network. It is also noteworthy that the RPGC naturally separates the dc, which allows us more freedom for optimum base and collector biasing. The harmonic power is collected at the base of the transistors for better harmonic generation efficiency. Compared with [15], slightly smaller transistors are chosen in this design to lower the fundamental oscillation in order to increase the locking range between the PLL and the radiator cells.

To increase the total radiated power, sixteen radiator cells are implemented to form a 4 × 4 array with their power combining constructively in the far field, as shown in Fig. 5. In each row, four radiator cells are mutually coupled together. The mutual coupling is realized through coupling transmission line tapping on the radiator self-feeding lines, as shown in Fig. 7. In [15], it has been shown that the radiator cells can only be coupled in phase, so the boundary between two adjacent cells behaves like an open termination. As a result, the added coupling lines act like small shunt capacitors. To minimize the impact, the coupling lines need to be short and have a high characteristic impedance. As a result, CPW lines with thin signal traces are used. Due to the compact design of the radiator cells, the 4 × 4 array only occupies an area of 0.87 × 0.85 mm². The simulated backside radiation patterns of a single radiator cell and the 4 × 4 array are shown in Fig. 8, with the directivities of 7.4 and 17.7 dBi, respectively.

B. 160 GHz Phase-Locked Loop

As shown in Fig. 5, the PLL is composed of a phase frequenter detector (PFD), a charge pump, a third-order loop filter, a divide-by-256 divider chain and four mutually coupled voltage-controlled oscillators (VCOs), as well as VCO fundamental buffers and harmonic buffers.

Since there is no strong coupling mechanism among the radiator rows, four mutually coupled VCOs are implemented to inject their second harmonic into each radiator row to obtain overall synchronization. The schematic of the VCO with the

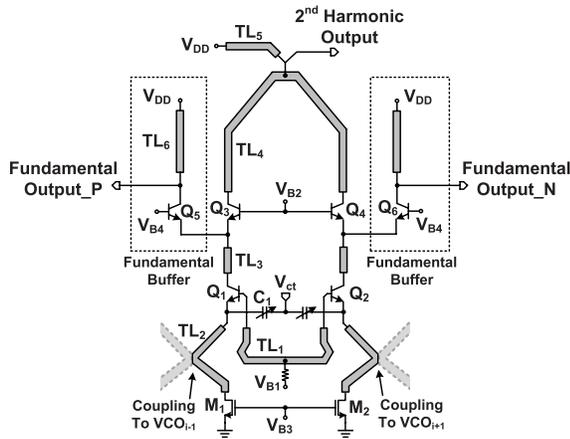


Fig. 9. Schematic of the VCO and the fundamental buffer.

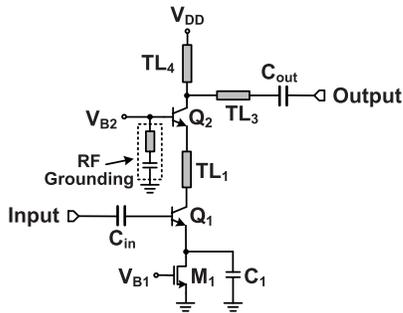


Fig. 10. Schematic of the VCO second-harmonic buffer.

fundamental buffer is shown in Fig. 9. As mentioned before, to assure frequency locking between the PLL and the radiator array, a large tuning range is required for the PLL. However, in conventional cross-coupled VCOs, the large transistor parasitic capacitance C_{π} is in parallel with the varactor, which makes it extremely hard to get a desired tuning range with adequate oscillation power due to the lossy varactor at this frequency. To obtain a better tradeoff, a differential Colpitts oscillator topology is adopted [15]. In the VCO, a common-base cascode stage (Q_3 and Q_4) is placed on top of the main transistors Q_1 and Q_2 to provide a low-impedance termination required by Colpitts oscillators. The second-harmonic signal is extracted at the top of the transmission line TL_4 , which will be sent to the second-harmonic buffer. The transmission line TL_2 is used to transform the large parasitic drain capacitance of M_1 and M_2 into a weakly inductive impedance, so the operation of the VCO is not affected. The intermediate node of TL_2 is directly connected to the adjacent VCO for a strong mutual coupling. Similar to the mutual coupling of the radiators, VCOs are coupled in phase and the connect points present open, so each VCO itself is not affected. The control signal (V_{ct} , shown in Fig. 5) is carefully distributed into the four VCOs to avoid frequency mismatch. Another common-base n-p-n transistor pair Q_5 and Q_6 with transmission lines on their collectors form the differential fundamental buffer, which feeds the 80 GHz output fundamental signal into the following divider chain (or dummy load, for minimizing frequency mismatch among the VCOs). Shown in Fig. 10 is the

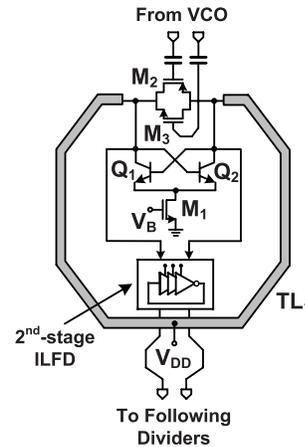


Fig. 11. Schematic of the ILFDs.

second-harmonic buffer, in which a cascode structure is used. A series L and C section is placed at the base of Q_2 , which resonates at 160 GHz to present a small impedance for RF grounding. Both input and output coupling capacitors (C_{in} and C_{out}) are custom designed metal-oxide-metal (MOM) capacitors to minimize the parasitic capacitance to the ground. According to simulation, -2.4 dBm power is injected into each radiator row from the second-harmonic buffer. It is worthy to mention that in steady state, the loading of the second-harmonic buffers will break the symmetry of the radiator rows. In order to minimize this impact, the buffers need to have large output impedances.

Shown in Fig. 11 is the schematic of the injection-locking dividers (ILFDs). The transmission line TL_1 and transistor pair Q_1 and Q_2 form the oscillator core of the first-stage ILFD. The free-running frequency is designed to be 40 GHz and can be tuned by changing the bias of the tail NMOS transistor M_1 in the case of process variation. The input signal is injected into the oscillator core through M_2 and M_3 . For the second-stage ILFD, the inverter-based ILFD topology is used for its compact size and wide locking range. Multiphase injection technique is also adopted to further increase the locking range [22]. Eventually, the overall input locking range of the ILFDs is determined by the first stage, which is simulated to be from 75 to 85.2 GHz, and is large enough to ensure locking of the whole PLL. The output of the ILFDs is sent to two cascaded CML dividers (from 20 GHz to 5 GHz) followed by a divide-by-16 digital divider made of TSPC logic (from 5 GHz to 312.5 MHz). The total division ratio of the divider chain is 256.

Finally, the simulated locking range of the PLL is around 17 GHz at the 160 GHz output, which is large enough to cover $\pm 5.3\%$ radiator frequency shift. This is very helpful for assuring frequency coherency even under large process variation.

IV. DESIGN OF THE HIGH-SENSITIVITY HETERODYNE DETECTION RECEIVER

To pair with the transmitter, a 320 GHz high-sensitivity subharmonic-mixing coherent receiver is designed, with the

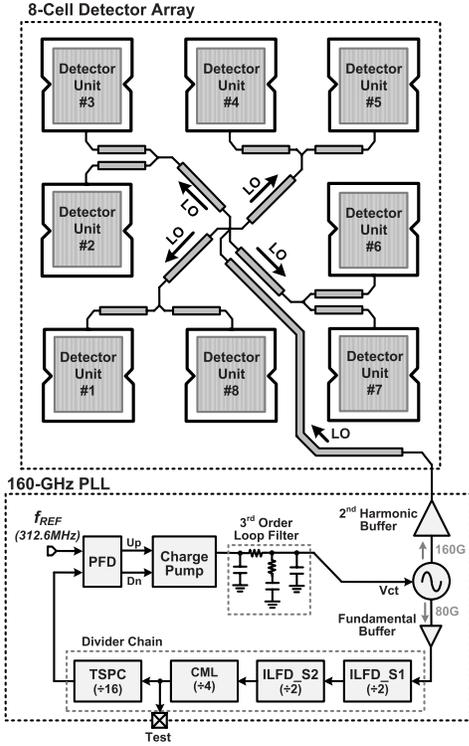


Fig. 12. Subharmonic-mixing heterodyne detection receiver architecture.

architecture shown in Fig. 12. It is composed of an eight-cell detector array, a 160 GHz PLL, and an LO distribution network. Using the subharmonic-mixing scheme, the output of the PLL is directly used as the LO signal. In this way, lower power consumption and a much wider LO tuning range are achieved. In this section, some design details will be discussed.

A. Subharmonic-Mixing Heterodyne Detector Cell

The structure of the proposed subharmonic-mixing heterodyne detector cell is shown in Fig. 13, in which bipolar transistors are used to perform the LO and RF mixing. The received RF signal is injected into the emitter of the transistors and the LO signal is fed from their base. The detector cell is made into a differential form in order to alleviate the LO self-mixing problem. After LO and RF mixing, the generated IF signal is amplified by a low-noise preamplifier before it gets mixed again into the 100 kHz baseband signal. Finally a low-pass filter with a 200 kHz cutoff frequency is followed to filter out the unwanted components.

To accommodate to the differential detector structure, a differential patch antenna is designed. The top and cross-sectional views of the antenna are shown in Fig. 14(a) and (b), respectively. The antenna occupies an area of $250 \times 240 \mu\text{m}^2$. The antenna is implemented using the top metal (M6), which has a thickness of $3 \mu\text{m}$. To avoid the terahertz wave from coupling into the lossy silicon substrate, an overlapped M1-to-M3 ground plane is placed underneath the antenna. The distance between the antenna to the ground plane is $7.61 \mu\text{m}$. To avoid crosstalking with the near-by structures (transmission lines, transistors, etc.), stacked M1-to-M6 metal walls are

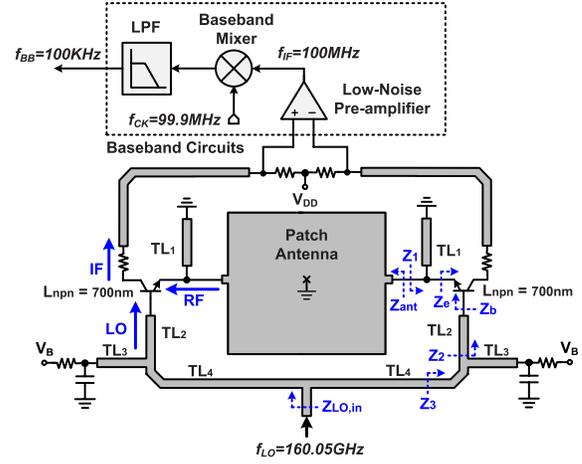


Fig. 13. Structure of the subharmonic-mixing heterodyne detector cell.

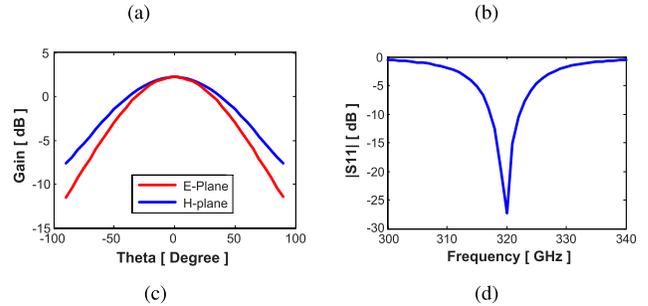
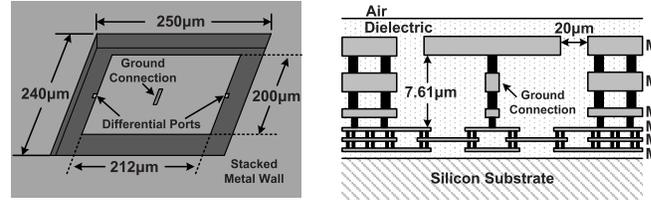


Fig. 14. Differential patch antenna. (a) Top view. (b) Cross section. (c) Simulated antenna gain in different directions. (d) Simulated reflection coefficient versus frequency ($Z_{in} = 350 \Omega$).

placed surrounding the antenna with a $20 \mu\text{m}$ clearance. Though the ground walls slightly degrade the efficiency of the antenna, adding them provides us with better prediction of the antenna resonance frequency, which is very important due to the narrow bandwidth of the patch antennas. As shown in Fig. 13, the emitter of the transistors is directly connected to the antenna. To provide a dc bias, the center of the patch antenna is connected to ground as shown in Fig. 14(a) and (b). Due to the differential structure, the central line of the antenna is equivalently RF grounded, so this ground connection has no impact. The length of the antenna is set to be $212 \mu\text{m}$ for a resonance at 320 GHz, and the width is designed to be $200 \mu\text{m}$ to obtain an impedance of 350Ω for easy matching with the input impedance at the emitter. The simulated antenna gain in different directions and the reflection coefficient versus frequency are shown in Fig. 14(c) and (d), respectively. The antenna gain in the broadside is simulated to be 2.2 dB.

To minimize the RF signal loss, the transistors are placed as close to the antenna as possible, with a very simple

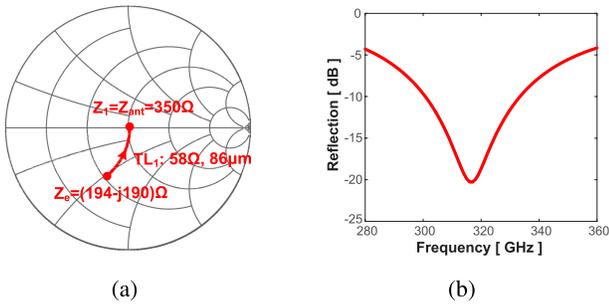


Fig. 15. RF matching at emitter. (a) Matching scheme on a Smith chart. (b) Simulated reflection coefficient versus frequency.

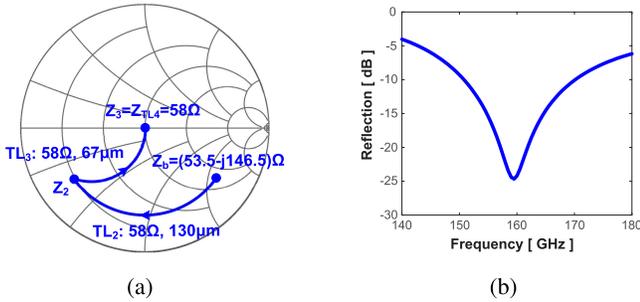


Fig. 16. LO matching at base. (a) Matching scheme on a Smith chart. (b) Simulated reflection coefficient versus frequency.

matching scheme: only one shunt transmission line stub (TL_1) is used as shown in Fig. 13. The matching scheme on a Smith chart is shown in Fig. 15(a). The $86 \mu\text{m}$ shunt stub TL_1 transforms the emitter impedance of $(194-j190) \Omega$ into 350Ω for matching with the patch antenna. To make this matching scheme feasible, a codesign is needed for the antenna and the transistors in order to obtain suitable impedances. Besides that, a tradeoff between the conversion loss and the device noise also needs to be considered while choosing the transistor size. The simulation result of the RF reflection coefficient at the transistor emitter (assuming a source impedance of 350Ω) is shown in Fig. 15(b). In the detector cell, all the transmission lines are made of G-CPW lines with a characteristic impedance of 58Ω . The matching scheme for the LO signal is shown in Fig. 16(a). The transmission line section TL_2 and the short matching stub TL_3 transform the capacitive transistor base input impedance into a 58Ω impedance, so that it is perfectly matched with the characteristic impedance of the feed line TL_4 . The dc bias for the base of the transistors is provided at the far end of TL_3 . Then, the feed lines (TL_4) on the two sides combine to form a common LO feed-in point, which has an input impedance ($Z_{\text{LO,in}}$) of 29Ω . The simulated LO reflection coefficient at this feed-in point (assuming a source impedance of 29Ω) is shown in Fig. 16(b).

B. 160 GHz Phase-Locked Loop

The PLL in the receiver is very similar to the one in the transmitter, but it has only one VCO, as shown in Fig. 12. In addition, high output impedance is no longer required for the VCO second-harmonic buffer, so it can be modified

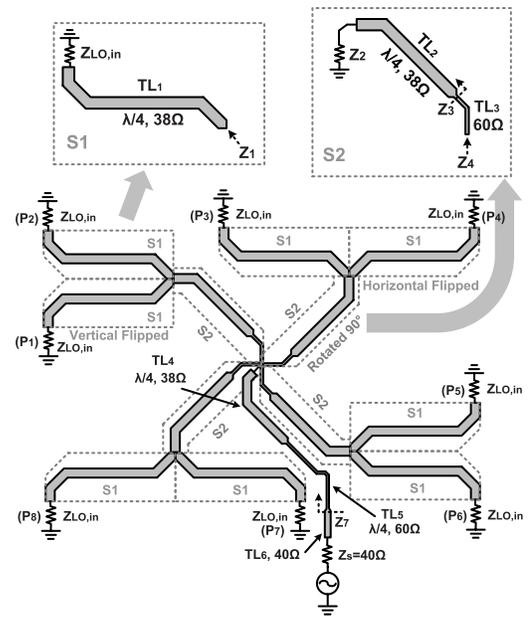


Fig. 17. Highly symmetrical LO distribution network structure.

to maximize the delivered LO power. The simulated output tuning range is 18.1 GHz at the 160 GHz output, which is slightly larger than the one in the transmitter.

C. Highly Symmetrical LO Distribution Network

As shown in Fig. 12, the LO signal generated by the PLL needs to be delivered into each of the eight detector cells. However, to distribute the LO power evenly with the same delay (phase) and power is challenging. In order to achieve that, a highly symmetrical distribution network shown in Fig. 17 is designed. First, the LO feed-in points of every two adjacent detector cells are combined together with two S1 blocks, forming four adjoint points. Then, four S2 blocks combine the four newly formed adjoint points together to get a common LO feed-in point for all the eight detector cells. Since the network is mainly built up upon S1 and S2 as well as their flipped and rotated versions, it is highly symmetrical, which is very helpful for the eight detector cells to receive an LO signal with the same power and phase.

In the S1 block, a 38Ω quarter-wave line transforms the 29Ω detector cell LO port impedance into a 50Ω impedance ($Z_1 = 50 \Omega$). After two adjacent detector LO ports are combined, the impedance seen from each of the adjoint points will be $Z_2 = Z_1/2 = 25 \Omega$. Then, in the S2 block, another 38Ω quarter-wave line TL_2 transforms Z_2 into a 60Ω impedance, so the length of the following 60Ω line TL_3 can be adjusted according to the desired distance between the detector cells. After the four S2 blocks join together, the impedance seen at the common LO feed-in point will be $Z_5 = Z_4/4 = 15 \Omega$. Then, a 38Ω and a 60Ω quarter-wave line (TL_4 and TL_5) further transform the impedance into 40Ω ($Z_7 = 40 \Omega$), as shown in Fig. 17. Assuming that 0 dBm signal power is applied at the input port of the distribution network, the simulated power and phase shift at all the eight output ports

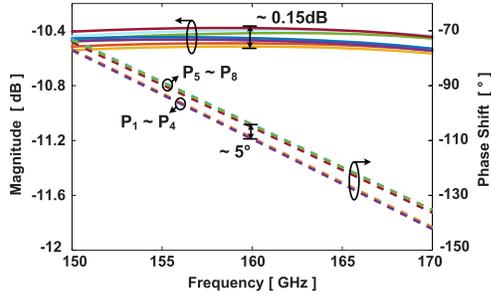


Fig. 18. Simulation results of the LO distribution network.

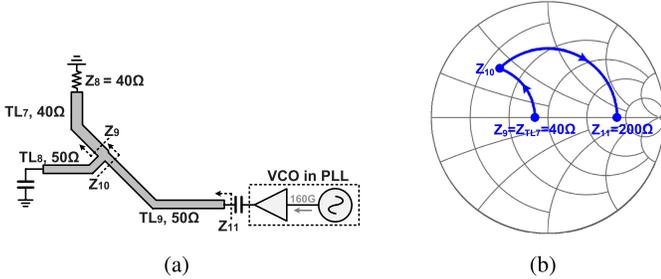


Fig. 19. Matching network at the output of the 160 GHz PLL. (a) Structure. (b) Matching scheme on a Smith chart.

are shown in Fig. 18. The LO power is evenly distributed with only a 0.15 dB difference among eight output ports. The total loss of this distribution network is 1.5 dB. Phase of the upper four outputs (P_1 – P_4 in Fig. 17) is around 5° behind the lower four outputs (P_5 – P_8), this is because the transmission line tapping to the center of the network (TL_4 in Fig. 17) slightly breaks the symmetry. Fortunately, this phase difference causes only a constant phase offset, which can be easily calibrated.

The simulated optimal load for the VCO harmonic buffer is 200Ω , so a short-stub matching structure is used to transform the 40Ω input impedance of the LO distribution network into 200Ω , as shown in Fig. 19. The 40Ω feed line between the LO distribution network and this matching structure can have an arbitrary length, providing more freedom for floorplan of the whole chip. Finally, the LO power delivered into each detector cell is simulated to be -12 dBm.

V. PROTOTYPE AND EXPERIMENTAL RESULTS

The proposed coherent imaging transceiver chips are fabricated using the STMicroelectronics 130 nm SiGe:C BiCMOS process. The transmitter chip shown in Fig. 20(a) occupies an area of 1.6×1.3 mm². The receiver chip shown in Fig. 20(b) takes an area of 1.7×1.8 mm².

A. Transmitter Measurements

Since the transmitter chip radiates from the backside, to eliminate the lossy substrate wave, a high-resistivity hemispherical silicon lens is used [21]. For ease of packaging and alignment, a high resistivity silicon wafer ($300 \mu\text{m}$ thick and ~ 1 cm² large) is placed in between the chip and the silicon lens [23]. The frequency/spectrum measurement setup is

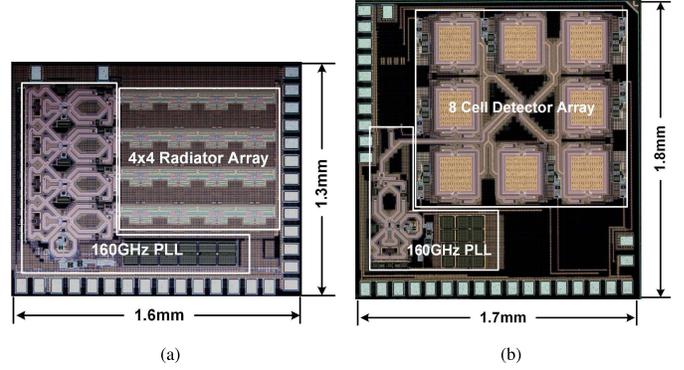


Fig. 20. Microphotograph of the (a) transmitter chip and (b) receiver chip.

shown in Fig. 21(a), in which an even harmonic mixer (EHM) mixes the received THz beam with the 16th harmonic of the 20 GHz signal supplied by the signal source. The IF product is then measured with the spectrum analyzer. The measured IF spectrum with the PLL on and off is shown in Fig. 22. When the PLL is off, there is no strong coupling among the radiator rows, multiple peaks are observed [Fig. 22(a)]. The number of the peaks does not equal to the number of the radiator rows, which is caused by the mutual pulling among the rows through the silicon substrate and antenna coupling. When the PLL is turned on, the radiator rows get synchronized through the mutually coupled VCOs and only a single peak is observed [Fig. 22(b)]. For a better comparison, a close-in spectrum of the free-running scenario and frequency locked scenario are plotted in the same graph, as shown in Fig. 23. It is obvious that after the frequency locking, the spectrum of the radiated THz beam is determined by the PLL, which presents a much sharper tone compared with the free-running case. The phase noise after the frequency locking is also shown in Fig. 23. Due to the large division ratio ($N = 1024$ from 312.5 MHz to 320 GHz) and the wide tuning range requirement for the PLL, the output phase noise is sacrificed. The measured in-band (100 kHz offset) and out-of-band (10 MHz offset) phase noises are -67.4 and -87.2 dBc/Hz, respectively. The frequency locking range of the transmitter under different radiator base bias voltages is shown in Fig. 24. As the bias voltage increases, the oscillation activity of the radiators also increases, and as discussed before, the locking range decreases quickly. However, a total locking range of 3.91 GHz is still achieved, which is largely improved compared with [15].

The radiation pattern of the transmitter shown in Fig. 25 is measured by rotating the chip in both azimuth and elevation directions on a rotary stage. The measured directivity is 18.0 dBi. It is noteworthy that the insertion of the silicon wafer makes the chip not exactly at the spherical center of the lens, which will lead to beam collimation. This explains why we observe lower side lobe level in Fig. 25 compared with the simulation in Fig. 8(b). However, due to the concentrated beam radiated by the radiator array, the measured directivity is still close to the simulation [23]. The power measurement setup is shown in Fig. 21(b), in which a PM4 calorimeter is used for better precision. To obtain accurate results, we need to make sure that the horn antenna is put far away enough from

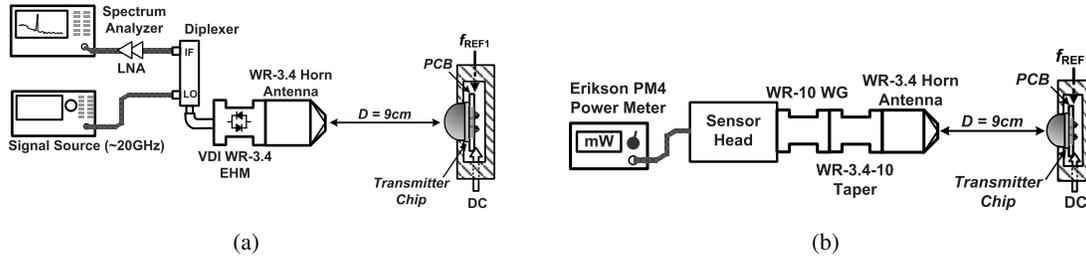


Fig. 21. Transmitter measurement setups. (a) Frequency/spectrum measurement setup. (b) Power measurement setup.

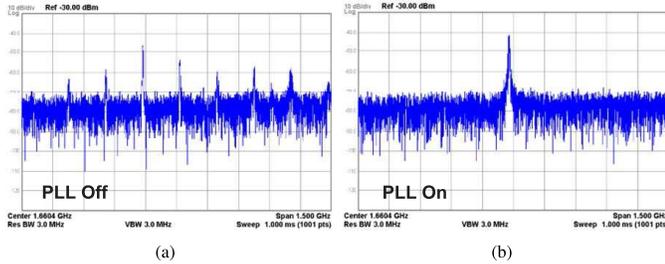


Fig. 22. Measured spectrum of the downconverted transmitter radiation when (a) PLL is off and (b) PLL is on.

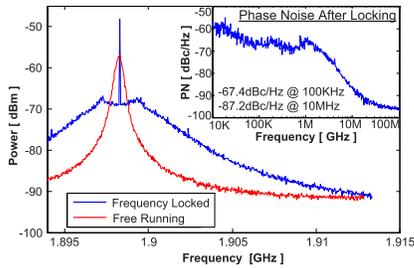


Fig. 23. Close-in free-running and frequency-locked spectrum of the downconverted transmitter radiated signal and the phase noise of it after frequency locking.

the transmitter to ensure far-field condition and avoid standing wave effect so that the Friis equation is valid. First, the distance is changed from 5 to 12 cm, the calorimeter measured power is shown in Fig. 26(a). It can be seen that when the distance is larger than 6 cm, the results match with the Friis equation well. In the following measurements, a 9 cm distance is chosen. The supply voltage for the transmitter is swept, and the peak radiated power and the associated dc-to-THz-radiation efficiency are shown in Fig. 26(b). The maximum radiated power and EIRP achieved are 2 mW and 21.1 dBm, respectively. The maximum dc-to-THz-radiation efficiency is 2.4%.

The transmitter chip consumes a total dc power of 605 mW: the radiator array dissipates 433 mW, the VCO array (including fundamental buffers and harmonic buffers) takes 128 mW, and the rest of the PLL consumes a 44 mW power.

B. Receiver Measurements

The measurement setup for the receiver is shown in Fig. 27. The transmitter chip works as the source to radiate the 320 GHz RF signal. To eliminate the standing wave

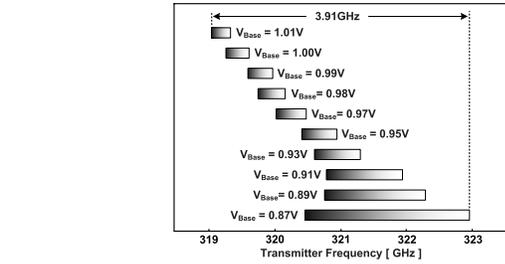


Fig. 24. Measured frequency locking range under different radiator bias points.

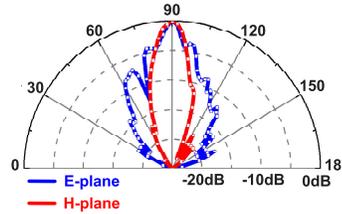


Fig. 25. Measured radiation pattern of the transmitter.

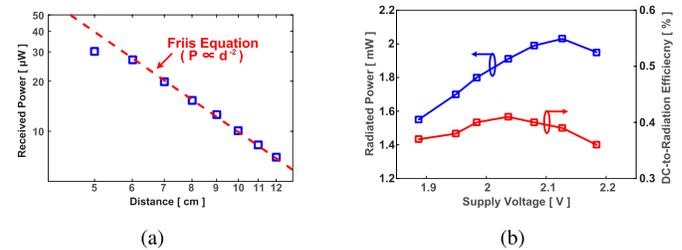


Fig. 26. Power measurement results. (a) Measured power by the calorimeter at different distances from the transmitter chip. (b) Measured peak output power and the associated dc-to-THz radiation efficiency under different supply voltages.

effect caused by reflection at the receiver PCB, an absorber is positioned in front of it with a hole for the wave to pass through. Even with the absorber, the receiver still needs to be put at least 15 cm away from the transmitter. The signal analyzer and the oscilloscope are used to observe the receiver output signal in frequency and time domains, respectively. Fig. 28 shows the measured phase noise of the CML output signal in the receiver PLL (test point in Fig. 12). Since it is the LO signal divided by 32, the phase noise of the LO is 30 dB higher. At a large offset frequency (>1 MHz), the

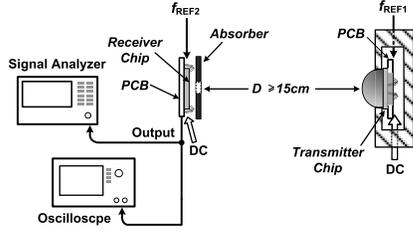


Fig. 27. Measurement setup for the receiver chip.

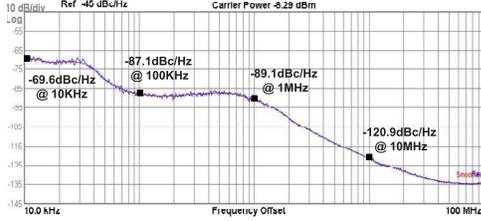


Fig. 28. Measured phase noise of the divided LO signal in the receiver.

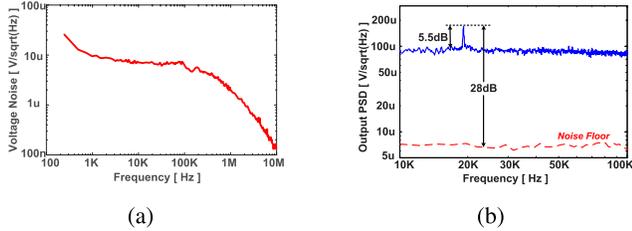


Fig. 29. Receiver chip measurement results. (a) Output voltage noise spectrum density. (b) Output signal power spectral density.

LO has a similar phase noise compared with the transmitter. However, at lower offset frequency (<100 KHz), the LO shows worse phase noise performance, which is caused by the inferior flicker noise of the reference clock used in the receiver. Using a signal analyzer, the output voltage noise spectrum density of one detector cell is measured with the transmitter chip turned off. As shown in Fig. 29(a), the noise density from 10 to 100 kHz is almost flat with a value of around $6.8 \mu V/\sqrt{\text{Hz}}$. Beyond 200 kHz, the noise starts to get filtered out by the baseband filter. With a 15 cm transmitter-to-receiver distance, the measured output signal PSD is shown in Fig. 29(b). Since the phase noise of both RF and LO will be transferred into the output after mixing, the close-in phase noise of the output is limited. As a result, the signal power is spread within the 90 kHz bandwidth. However, due to the high sensitivity of the detector cells, the output still has a peak 28 dB higher than the noise floor. To get better use of the output signal power, it is integrated from 10 to 100 kHz to get an output rms voltage. The output rms voltage as well as the detector cell received RF power at different distances is shown in Fig. 30(a). A -20 dBV/dec slope is observed for the output rms voltage, which matches the theory of heterodyne detection and is different from the -40 dBV/dec slope observed in conventional incoherent detectors [24]. This is one of the factors that give rise to much higher sensitivity

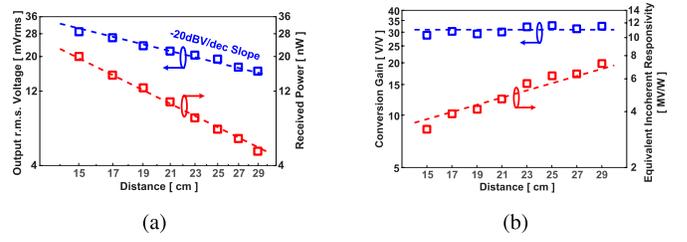


Fig. 30. Measured receiver (a) output rms voltage as well as the received RF power at different transmitter-to-receiver distances and (b) conversion gain as well as equivalent incoherent responsivity at different transmitter-to-receiver distances.

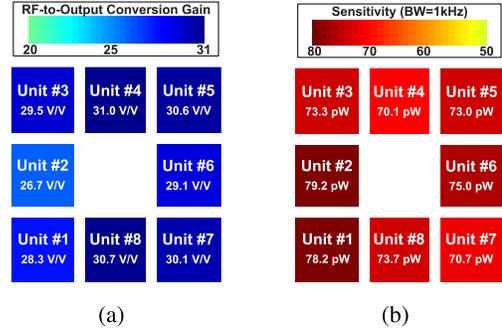


Fig. 31. Performances of all the eight detector cells. (a) Conversion gain. (b) Sensitivity under 1 kHz bandwidth.

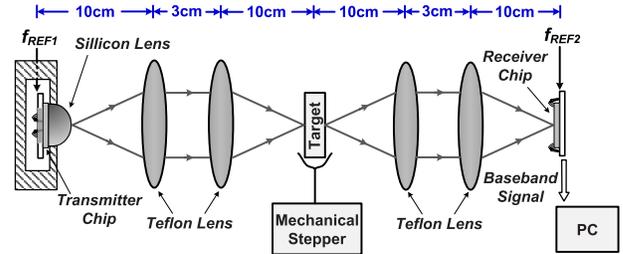


Fig. 32. Imager setup using the proposed transceiver chips.

for the heterodyne detectors. There are two ways to obtain the detector cell received RF power. The first method is to use the setup in Fig. 21(b) to measure the power density at a certain distance and then calculate the power P_r a detector cell could receive if the receiver chip is positioned there

$$P_r = \frac{P_{\text{cal.}}}{A_{\text{horn}}L} A_{rx} = \frac{P_{\text{cal.}}}{G_{\text{horn}}L} G_{rx} \quad (3)$$

where $P_{\text{cal.}}$ is the measured power with the calorimeter, A_{horn} and G_{horn} are the aperture size and gain of the horn antenna used, respectively, L is the loss of the additional WR-10 section and WR-10-3.4 taper, and A_{rx} and G_{rx} are the aperture size and gain of the receiver on-chip patch antenna, respectively. The second way is to use the Friis equation to calculate the RF power one detector cell can receive

$$P_r = \frac{P_{\text{out,tx}} D_{\text{tx}}}{4\pi d^2} A_{\text{patch}} = \left(\frac{\lambda}{4\pi d}\right)^2 P_{\text{out,tx}} D_{\text{tx}} G_{rx} \quad (4)$$

where $P_{\text{out,tx}}$ and D_{tx} are the output power and directivity of the transmitter, respectively, d is the transmitter-to-receiver

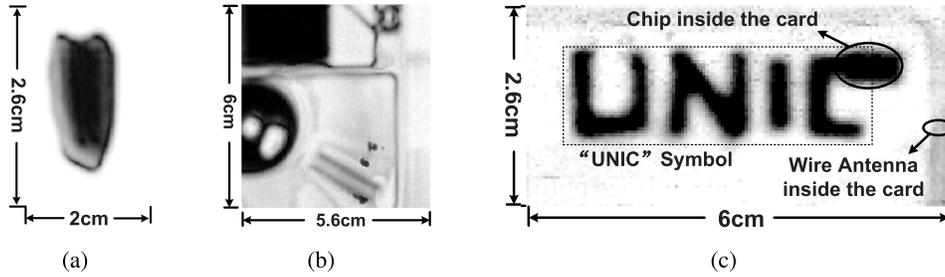


Fig. 33. Images formed by the imager using the proposed transceiver. (a) Human tooth (130 × 80 pixels). (b) Floppy disk (150 × 140 pixels). (c) Student ID card with a metallic “UNIC” symbol attached to it (150 × 66) pixels.

distance, and G_{rx} is the gain of the receiver antenna. In our measurement, we adopted the first method and verified the results with the second method. The results are consistent with only minor differences. Assuming a 50 Ω impedance for the RF signal, a conversion gain from the received RF rms voltage to output rms voltage can be calculated using

$$G_v = \frac{V_{rms}}{\sqrt{P_r \cdot 50 \Omega}} \quad (5)$$

where V_{rms} is the output rms voltage and P_r is the received RF power. The conversion gain at different distances is shown in Fig. 30(b). The averaged conversion gain is 31.0 V/V. To compare with incoherent detectors, an equivalent incoherent responsivity is defined as the responsivity that an incoherent detector needs to generate the same output rms voltage with the same received RF power. This equivalent responsivity can be derived with [24]

$$\mathfrak{R}_v = \frac{\pi V_{rms}}{\sqrt{2P_r}} \quad (6)$$

The receiver equivalent responsivity at different distances is also shown in Fig. 30(b). It is observed that as the received power decreases, the receiver equivalent incoherent responsivity increases. This also reflects the effectiveness of enhancing detection sensitivity using heterodyne detection. To make a fair comparison between coherent and incoherent imagers, a sensitivity is defined as the received RF power for the output signal to have SNR = 1 within a 1 kHz bandwidth (corresponding to 1 ms time constant for fast imaging). The sensitivity of the proposed receiver is calculated to be 70.1 pW, which is around ten times better compared with other state-of-the-art silicon detectors (as shown in Table III). The sensitivity enhances even further with a larger bandwidth (about 20 times for 10 kHz bandwidth and 70 times for 100 kHz bandwidth) corresponding to faster imaging. The measured conversion gain and sensitivity for all the eight detector cells are shown in Fig. 31. Thanks to the highly symmetrical LO distribution network, the performances of the detector cells are quite uniform.

C. Imager Experiments

To put the transceiver into real use, a transmission mode terahertz imager is built up as shown in Fig. 32, which is composed of the transceiver chips, four Teflon lenses, and a mechanical stepper. The first two Teflon lenses are used to

TABLE I
PERFORMANCE SUMMARY OF THE TRANSMITTER

| | |
|---------------------------------|---|
| Output Frequency Range | 319.04 ~ 322.95 GHz |
| Peak Radiated Power | 2 mW |
| EIRP | 21.1 dBm |
| Directivity | 18.0 dBi |
| Peak Radiator Efficiency | 0.41 % |
| Phase Noise | -67.4 dBc/Hz @ 100KHz offset -66.8 dBc/Hz @ 1MHz offset -87.2 dBc/Hz @ 10MHz offset |
| DC Consumption | 433 mW (Radiator Array) 172 mW (PLL) |

TABLE II
PERFORMANCE SUMMARY OF THE RECEIVER

| | |
|---|---|
| LO Tuning Range | 152.5 ~ 164.8 GHz |
| Antenna Gain | 2.2 dB |
| Output Voltage Noise | 6.7 μ V/ \sqrt{Hz} @ 100KHz |
| RF-to-Output Conversion Gain | 31.0 V/V |
| Equivalent Incoherent Responsivity | > 7.26 MV/W |
| Sensitivity¹ | 70.1 pW |
| DC Consumption | 41.6 mW (Detector Array) 75.5 mW (PLL) |

1. At an assumed bandwidth of 1 kHz.

focus the terahertz beam generated by the transmitter chip and form a focal plane. The two Teflon lenses on the receiver side are used to refocus the transmitted beam in order to increase the power that could be received by the receiver chip. The mechanical stepper is used to move the object on the focal plane for scanning. With this imager, a few terahertz images are formed, as shown in Fig. 33.

VI. CONCLUSION

The performances of the proposed transmitter and receiver chip are summarized in Tables I and II, respectively. The transmitter chip achieves a peak radiated power of 2 mW and a peak EIRP of 21.1 dBm with a total dc power consumption of 605 mW. The receiver chip achieves an equivalent incoherent responsivity of more than 7.26 MV/W and a sensitivity of 70.1 pW under an integration bandwidth of 1 kHz. The total dc power consumption of the receiver chip is 117 mW. A comparison with other terahertz imagers is given in Table III. It can be seen that under the 1 kHz integration bandwidth, the proposed coherent imager can achieve around

TABLE III
COMPARISON WITH PREVIOUS STATE-OF-THE-ART WORKS

| References | Technology | Frequency | Array Size | Responsivity | Sensitivity ⁶ | Coherent Sensing |
|------------------|-------------|-----------|--------------|-------------------------|--------------------------|------------------|
| [9] | 130-nm CMOS | 0.28 THz | 4×4 | 336 V/W ¹ | 917 pW ⁷ | No |
| | | 0.86 THz | single pixel | 273 V/W ¹ | 1.33 nW ⁷ | |
| [10] | 180-nm SiGe | 0.32 THz | 4×4 | 18 kV/W ² | 1.08 nW ⁷ | No |
| [11] | 65-nm CMOS | 0.86 THz | 32×32 | 140 kV/W ³ | 3.16 nW ⁷ | No |
| [18] | 130-nm SiGe | 0.26 THz | 4×4 | 2.6 MV/W ⁴ | 250~278 pW ⁷ | No |
| This Work | 130-nm SiGe | 0.32 THz | 8 cell array | >7.26 MV/W ⁵ | 70.1 pW ⁷ | Yes |

1. 24 dB on-chip amplifier gain is de-embedded.
2. 22 dB amplifier/buffer gain included.
3. On-chip readout circuit gain and 5 dB off-chip VGA gain included.
4. 33~57.5 dB VGA gain included.
5. The equivalent responsivity of the coherent detector is defined as: the responsivity an incoherent detector needs to generate the same output rms voltage with the same received power level. 60 dB baseband gain included.
6. The sensitivity is defined as the input power level for the output signal to have SNR=1 within 1 kHz bandwidth.
7. Assume noise spectrum density is flat within the 1 kHz bandwidth.

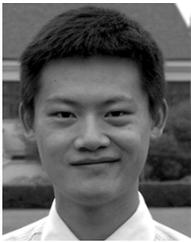
ten times better sensitivity compared with other state-of-the-art incoherent ones. Using the PLL-based architecture, no off-chip high-frequency high-power sources are needed. To our best knowledge, this paper demonstrates the first fully integrated coherent terahertz imaging transceiver on silicon.

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Chen Jiang (S'15) received the B.Sc. and M.Sc. degrees in microelectronics from Fudan University, Shanghai, China, in 2010 and 2013, respectively. In 2013, he joined the Ultra-high-speed Nonlinear Integrated Circuits Lab, Cornell University, Ithaca, NY, USA, where he is currently pursuing the Ph.D. degree.

Since 2016, he has been a Visiting Scholar with the University of Michigan, Ann Arbor, MI, USA. His current research interests include novel millimeter-wave and terahertz electronics for imaging, sensing, and communication applications.

Mr. Jiang is a member of the IEEE Solid-State Circuits Society. He was a recipient of Irwin and Joan Jacobs Fellowship, and the Sporcak Analog Design Fellowship, Cornell University, in 2013 and 2014, respectively.



Ali Mostajeran (S'15) received the B.Sc. degree in electrical engineering from the Isfahan University of Technology, Isfahan, Iran, in 2011, and the M.Sc. degree in microelectronics from the Sharif University of Technology, Tehran, Iran, in 2013. He is currently pursuing the Ph.D. degree in electrical engineering with Cornell University, Ithaca, NY, USA.

He joined the Ultra-high-speed Nonlinear Integrated Circuits Lab, Cornell University. He is currently a Visiting Scholar with the University of

Michigan, Ann Arbor, MI, USA. His current research interests include millimeter-wave and terahertz circuits and systems design for hydration sensing and imaging applications, oscillator phase noise modeling, and optimization and improvement techniques.



Ruonan Han (S'10–M'14) received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2007, the M.Sc. degree in electrical engineering from the University of Florida, Gainesville, FL, USA, in 2009, and the Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2014.

In 2012, he was an Intern with Rambus Inc., Sunnyvale, CA, USA, where he was involved in designing energy-efficient I/O circuits. He is

currently the E.E. Landsman (1958) Career Development Assistant Professor with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA. His current research interests include microelectronic circuits and systems operating at millimeter-wave and terahertz frequencies for novel sensing and ultra-high-speed communications.

Dr. Han is a member of the IEEE Solid-State Circuits Society and the IEEE Microwave Theory and Techniques Society. He was a recipient of the Cornell ECE Director's Ph.D. Thesis Research Award, the Cornell ECE Innovation Award, and the Best Student Paper Award of the 2012 Radio-Frequency Integrated Circuits Symposium. He was also a recipient of the Irwin and Joan Jacobs Fellowship, the John M. Olin Fellowship, the IEEE Microwave Theory and Technique Society Graduate Fellowship Award, and the IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award.



Mohammad Emadi received the B.Sc. degree from the University of Tehran, Tehran, Iran, in 2004, and the M.Sc. and Ph.D. degrees in electrical engineering from the Sharif University of Technology, Tehran, Iran, in 2006 and 2012, respectively.

He was a Lead Designer with the Communication Systems Group, Sharif University Research Center, for six years, where he was involved in the development of wireless communication links and sensors using phased array antennas. He founded his first company, Sanat Sharif. He was a Manager with the Tolou Research Center, Sharif University, from 2011 to 2012. From 2013 to 2014, he was a Post-Doctoral Research Associate with the Ultra-High-speed Nonlinear Integrated Circuit (UNIC) Lab, Cornell University, Ithaca, NY, USA, where he was involved in sub-millimeter wave imaging systems especially for health care applications. He is currently with Qualcomm Inc., San Jose, CA, USA, as a Senior Staff Researcher, where he is involved in WiFi and small cell communication links. He also continues his previous research on terahertz medical systems with UNIC Lab. He has authored over 50 papers and patents in communication systems.

Dr. Emadi is a member of over ten academic and industrial committees. He received the Best Researcher of 2009 from the Ministry of Science, and the Silver Medal of the Physics Olympiad in 1999, and was honored at the IEEE Paper Contest, Iran, in 2004. He received the Cornell Electrical and Computer Engineering Innovation Award from Cornell University.



Hani Sherry (S'09–M'13) received the B.Sc. degree in computer and communication engineering from the University of Balamand, Lebanon, in 2006, and the M.Sc. degree in microwave and communication engineering from the School of Electrical and Electronic Engineering, The University of Manchester, and the Ph.D. degree in 2013. His Ph.D. thesis (*magna cum laude*) was on millimeter-wave and terahertz integrated circuits and systems with co-tutelle with the IHCT University of Wuppertal, Wuppertal, Germany, and IEMN/ISEN, Lille, France, and funded by STMicroelectronics, Crolles, France.

He joined the School of Electrical and Electronic Engineering, The University of Manchester, in 2007. He fulfilled a research dissertation with distinction on millimeter-wave noise characterization of HEMTs and MESFETs. In 2008, he joined O2-Telefonica, London, U.K., as a Radio Engineer and he was responsible for the 2G/3G network cell-planning and optimization for the East-London Region. He has been with STMicroelectronics, where he is currently a Senior Research Engineer on the advanced Research and Development topic of terahertz circuits and systems for multiple application fields. He has co-authored several international publications and patents. His current research interests include millimeter-wave and terahertz integrated circuits and systems for safety, security, and biomedical applications, and ultrahigh-speed wireless communications.

Dr. Sherry was a recipient of the ISSCC 2012 Jan Van Vessel Award for Outstanding European Paper for the work on a 1k-pixel terahertz video camera. In 2012, he was also a co-recipient of the STMicroelectronics Technology Council Innovation Prize.



Andreia Cathelin (M'04–SM'11) started her electronic studies at the Polytechnic Institute of Bucharest, Bucharest, Romania, and graduated from the Institut Supérieur d'Electronique du Nord (ISEN), Lille, France, in 1994. In 1998 and 2013, respectively, she received the Ph.D. and “habilitation a diriger des recherches” (French highest academic degree) degrees from the Université de Lille 1, France.

In 1997, she was with Info Technologies, Gradignan, France, where she was involved in analog and RF communications design. Since 1998, she has been with STMicroelectronics, Crolles, France, where she is currently with the Embedded Processing Solutions Segment, Technology Research and Development, as a Senior Member of the Technical Staff. She has authored or co-authored 100 technical papers and four book chapters, and filed over 25 patents. Her current research interests include the area of RF/mmW/THz systems for communications and imaging.

Dr. Cathelin is serving on several IEEE conferences and committees. She is an elected member of the IEEE SSCS Adcom from 2015 to 2017. She has been active at ISSCC since 2011. In 2011, she was a TPC member and the RF Sub-Committee Chair from 2012 to 2015. She is currently the Forums Chair and a member of the Executive Committee. She has been a member of several Technical Program Committees: VLSI Symposium on Circuits since 2010. She has been serving as the Officer and ESSCIRC since 2005. Since 2013, she has been on the Steering Committee of the ESSCIRC-ESSDERC conferences, where she is currently serving as the Vice-Chair. She is a member of the experts' team of the French Evaluation Agency for Research and Higher Education. She was a co-recipient of the ISSCC 2012 Jan Van Vessel Award for Outstanding European Paper and of the ISSCC 2013 Jack Kilby Award for Outstanding Student Paper, and winner of the 2012 STMicroelectronics Technology Council Innovation Prize.



Ehsan Afshari (S'98–M'07–SM'11) was born in 1979. He received the B.Sc. degree in electronics engineering from the Sharif University of Technology, Tehran, Iran, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology, Pasadena, CA, USA, in 2003 and 2006, respectively.

In 2006, he joined the Faculty of Electrical and Computer Engineering, Cornell University, Ithaca, NY, USA, as an Assistant Professor, and was promoted to Associate Professor in 2012. In 2016, he joined the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI, USA, as an Associate Professor. His current research interests are mm-wave and terahertz electronics and low-noise integrated circuits for applications in communication systems, sensing, and biomedical devices.

Dr. Afshari serves as the Distinguished Lecturer of the IEEE Solid-State Circuits Society and a member of the Technical Program Committee of the IEEE Radio Frequency Integrated Circuits Symposium. He was the Chair of the IEEE Ithaca Section, the Chair of the Cornell Highly Integrated Physical Systems, a member of the International Technical Committee of the IEEE Solid-State Circuit Conference, a member of the Analog Signal Processing Technical Committee of the IEEE Circuits and Systems Society, a member of the Technical Program Committee of the IEEE Custom Integrated Circuits Conference (CICC), and a member of the Technical Program Committee of the IEEE International Conference on Ultrawideband. He was a recipient of the National Science Foundation CAREER Award in 2010, the Cornell College of Engineering Michael Tien Excellence in Teaching Award in 2010, the Defense Advanced Research Projects Agency Young Faculty Award in 2008, and Iran's Best Engineering Student Award by the President of Iran in 2001. He was also a recipient of the best paper award in the CICC 2003, the first place prize at the Stanford–Berkeley–Caltech Inventors Challenge in 2005, and the Best Undergraduate Paper Award at the Iranian Conference on Electrical Engineering in 1999. He was a recipient of the Silver Medal in the Physics Olympiad in 1997, and a recipient of the Award of Excellence in Engineering Education from the Association of Professors and Scholars of Iranian Heritage in 2004.