Jack W. Holloway,
Georgios C. Dogiamis,
and Ruonan Han

Innovations in Terahertz Interconnects

The continued increase in computing capability that has occurred through the technology scaling foretold by Moore [1] and Dennard et al. [2] has led to a commensurate increase in the input–output requirements of computing systems. This phenomenon has been most significantly experienced in terms of the interconnect technologies in large data centers (DCs) and high-performance computing (HPC) applications. Historical data have shown a two to three times increase in aggregate data rates every two years [3]. This space covers a variety of different interconnect length scales. In a comprehensive survey by Thraskias et al. [4], high-speed interconnects are grouped according to the following taxonomy.

1) *Rack-to-rack*: Interconnects in this range, from a few meters to hundreds of meters, are presently served through a variety of high-speed optical and midspeed electrical (such as Ethernet and InfiniBand) interconnect technologies.
2) *Board-to-board*: Within a given rack, shorter-range electrical interconnects are utilized. These technologies are designed to address efficient, high-speed transport from tens of centimeters to a few meters.
3) *Module-to-module*: Interconnects on the scale of several to tens of centimeters address high-speed connections across backplanes, cards, and so forth.
4) *Chip-to-chip*: Technologies in this group generally address communication across a backplane or within a larger multichip module. They are on the order of a few centimeters. Examples include double data rate as well as ESIstream and JESD204 for high-speed parallel analog-to-digital interfaces.
5) *Core-to-core*: High-speed signaling among individual processor cores and memory in a system-in-package or a multichip module is handled via interconnects across a short range of a few to tens of millimeters. Examples include Intel's Embedded Multi-Die Interconnect Bridge.

Jack W. Holloway (holloway@mit.edu) and Ruonan Han (ruonan@mit.edu) are with the Massachusetts Institute of Technology, Cambridge. Georgios C. Dogiamis (georgios.c.dogiamis@intel.com) is with Intel Corporation, Components Research, Santa Clara, California.

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All of these applications are presently dominated by optical and electrical interconnects. As discussed in [4]–[6], the attenuation and dispersion associated with copper-based electrical interconnects led to an ever-increasing challenge to achieve both higher data rates and longer reaches. One example can be observed from the road map for Ethernet over copper-based channels [7]: although the data rates are doubling every three to four years, the maximum reach is reduced by half, thus resulting in a relatively constant bandwidth-distance product. To some extent, the frequency-dependent loss can be addressed through the use of transmitter preemphasis, receiver equalization, and forward error correction techniques, and larger waveguide or transmission line loss can be compensated for by signaling with higher power. These, however, inevitably reduce link efficiency and increase latency, with equalization becoming increasingly difficult at higher signaling bandwidth. As a result, increasing the data rate per lane in electrical links becomes more difficult for long-reach applications. High-order pulse-amplitude modulation is being adopted to keep the signal bandwidth low. For short-reach applications, such as interchip/core and small backplane communications, copper interconnects with high parallelism and density (terabits per second per millimeter) still serve well to provide high throughput, thanks to the low cost and small footprint of the links as well as their full compatibility with silicon infrastructure.

In comparison to copper, optical channel media exhibit excellent loss characteristics and substantially more available channel bandwidth. These advantages have led to ubiquitous adoption of long-haul fiber links with tera-scale aggregate data rate. However, the use of various sources and electrooptical components fabricated with III–V semiconductors renders the integration with commodity silicon processes difficult and expensive. In addition, the reliance of the operation on stabilized environmental temperature and high-precision component alignment degrades the reliability and further increases maintenance cost. It should be noted that significant research and development efforts have been focused on improving the efficiency of optical links below a meter, and the associated link efficiency and bandwidth density with more efficient lasers and electrooptical modulation schemes start to make the links competitive with their electrical counterparts [4]. Nevertheless, due to the aforementioned problems, optical links are still better suited for low-density, interrack connections across tens to hundreds of meters in HPC and DCs.

Although both long (tens of meters and above) and short (tens of centimeters and below) links are being well addressed, the gap between the two regimes provides an opportunity to investigate high-performance and low-cost alternatives. In this class of links, meter-level interconnects for neighboring server racks and backplanes are required to transport data at hundreds of gigabits per second per lane and high link densities. This interblade and backplane regime is in critical need of performance improvement and cost reduction (Figure 1). That is where we believe terahertz (i.e., 0.1- to ~1-THz) signals, generated and manipulated by electrical silicon chips and then transmitted over dielectric waveguides (Figure 2), may play a promising role.

Recently, there has been growing interest in research related to these types of concepts. Gu discussed the applications of waveguide-confined terahertz for communications and the concept's comparisons with all-electrical and optical interconnect and enumerated a number of the challenges associated with realizing such a link utilizing a single RF channel per waveguide [6]. The overall architecture shown in Figure 2 has a number of similarities to the multiband RF interconnect concept advanced by Chang et al. at the University of California, Los Angeles [8]–[10], in which multiple narrow-band data streams are multiplexed onto a conductive transmission medium. In this case, the very broad bandwidth, low losses, and smaller guide cross section associated with terahertz waveguides are utilized.

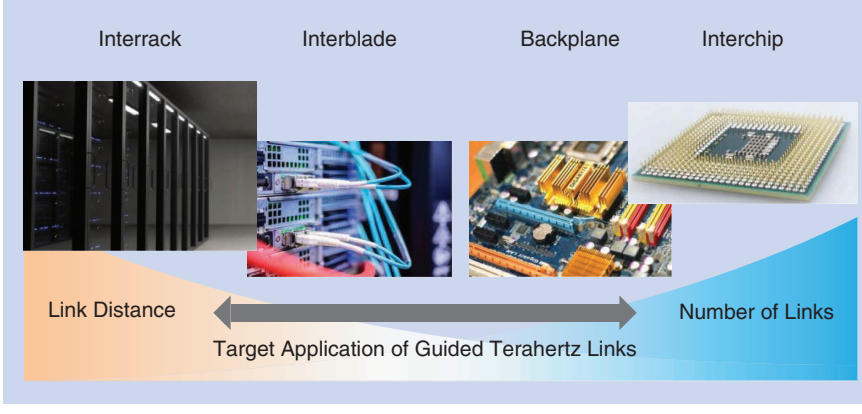

Figure 1. *An opportunity for the insertion of a high-data-rate, efficient, and cost-effective guided terahertz interconnect into an existing ecosystem of optical and electrical interconnects.*

Previously, applications of terahertz components have centered around radio astronomy, noninvasive imaging, molecular structure studies, and wireless communications [11]–[13]. During the past decade, developments of terahertz electronic components, especially those on commercial CMOS/BiCMOS chips, have made significant progress and

are making guided-terahertz communication (Figure 2) practical and affordable using existing silicon infrastructures. In addition, a variety of studies have been done to understand the material, waveguide, and supported modes' impact to transmission and dispersion in the terahertz and subterahertz regimes, just as in the fiber-optics community [14]. Although there has been some work on designing terahertz waveguides for low loss and low dispersion [15]–[19], more work needs to be done to demonstrate achievable dispersion at the lower terahertz or sub-millimeter-wave (mm-wave) frequencies addressed by silicon circuits. Achieving lower dispersion has an important impact on overall link performance by significantly reducing the complexity, power, cost, and latency associated with equalization schemes.

Operating at lower frequencies than optical solutions also provides additional robustness to waveguide misalignment. Due to the difference in operating wavelength, one expects a terahertz interconnect to demonstrate a few orders of magnitude more misalignment tolerance than an optical scheme. This would allow low-cost, misalignment-tolerant cable connections, which is one key for the cost reduction of the overall system. Furthermore, the cable itself, i.e., the terahertz waveguide, is targeted to be manufactured using similar low-cost techniques as those used for twinaxial cables, for example. The packaging required for the system is neither custom nor out of exotic materials or processes. This is yet another aspect that would lead to further system cost reduction. Hence, this link technology offers the promise of an end-to-end solution that will keep costs low from every perspective, while enabling excellent data rate and efficiency performance.

Enabling Technologies

Recent developments in terahertz materials, components, active semiconductor devices, packaging processes, and circuit techniques are paving the way toward a high-speed-per-lane, energy-efficient interconnect in the meter range, based on modulated and waveguide-confined terahertz waves. In this section, a few enabling technologies are introduced and analyzed.

Terahertz Dielectric Waveguides

Subterahertz and terahertz waveguides with waves confined in dielectrics, although more lossy (~1 to ~10 dB/m) than fiber-optic cables, provide significant attenuation improvements over electrical channels with similar bandwidth (>100 GHz) [16], [20]–[24]. Even at lower frequencies, there is a stark contrast in the loss characteristics of a dielectric waveguide and existing copper backplanes. In [25], a hollow tube is examined at V band and demonstrates 90–180-dB lower loss than a 1-m copper backplane. These advantages increase with higher operating frequencies where copper conductor-associated losses continue to increase.

In addition, the employed dielectric materials, usually consisting of amorphous polymer dielectrics, are relatively low cost. These materials can be processed using low-cost manufacturing techniques and are often compatible with existing printed circuit board (PCB) technologies.

The published works to date have studied a variety of waveguide materials and geometries [6], [16], [20]–[24]. These include a number of different waveguide cross sections—hollow cylindrical, solid cylindrical, fiber bundles, and rectangular waveguides. Each of these geometries supports a number of different spatial modes with varying single-mode operating frequencies. In addition, given the wavelength of operation in the terahertz regime (between 0.3 and 3 mm) and spatial constraints imposed by the platform architecture, one can consider the realization of both subwavelength and wavelength-scale cross sections. This decision can have significant impact on associated radiative and mode-coupler loss as well as dispersion. The survey carried out by Atakaramians et al. [14] is an excellent resource that discusses the tradeoffs associated with the design of waveguides (e.g., shapes, sizes, and material properties). This is a very rich area offering a large number of different waveguide types that may be considered depending on the application requirements.

Following our work in [5], the discussion here will focus on subwavelength waveguides with rectangular cross sections, because these lower the barrier to planar

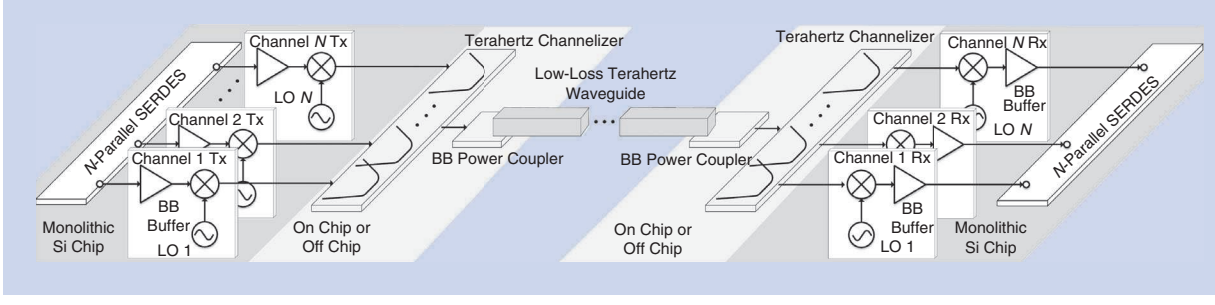

Figure 2. *A generalized parallel architecture to realize high-data-rate digital communication utilizing a rectangular dielectric terahertz waveguide. BB: broadband; Rx: receiver; SERDES: serializer/deserializer; Tx: transmitter; Si: silicon; LO: local oscillator.*

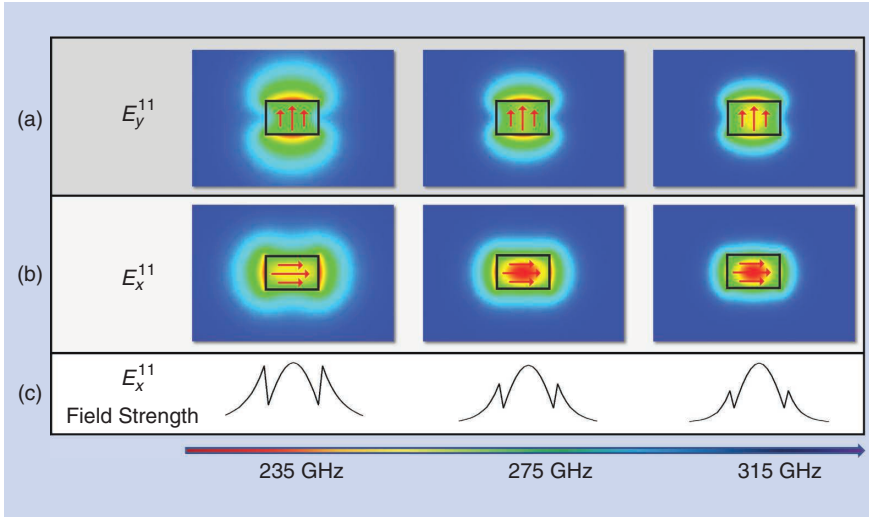

Figure 3. *A simulated mode confinement in a rectangular dielectric waveguide at varying frequencies. This waveguide has a 250 × 400 μm² cross section and is made from Rogers R3003 dielectric material. The (a) vertically and (b) horizontally polarized quasi-transverse electric modes are shown at various frequencies in H band. One can see that the modal profile remains consistent. (c) demonstrates that a larger proportion of the modal energy is contained within the waveguide itself at higher frequencies (in this case, the horizontally polarized mode).*

integration [5], [26] and can be readily manufactured either by laser-cutting existing sheets of bulk material or by direct polymer extrusion. Moreover, the technique provides (with the proper choice of material properties, operating band, and dimensions) separate quasi-horizontally and quasi-vertically polarized modes in the form of lower-order hybrid modes [5], [27], [28] (see Figure 3). The choice of a subwavelength geometry itself means that the guided terahertz wave is contained both within and outside of the guide material. The extent of the energy distribution beyond the waveguide surface is largely a function of the waveguide material dielectric constant ϵ_r and the guide dimensions. Figure 3 shows an example of this type of dielectric waveguide, which demonstrates the mode confinement around the guide. In addition, the figure illustrates the large bandwidth over which a given mode maintains its spatial profile. In this case, more than 100 GHz of single-mode operating bandwidth is available from 220 to 330 GHz, covering the entire H band.

Due to the modal distribution exhibited by these types of guides, undesired guide-to-guide coupling can occur for parallel guide geometries. This could be particularly significant in the case of meter-range interconnects and have a negative impact on the overall link performance. Undesired energy coupled from one waveguide into an adjacent waveguide manifests itself as uncorrelated interference or noise, thus reducing the effective signal-to-noise ratio (SNR) at the receiver. The isolation between two rectangular dielectric guides is illustrated in Figure 4, following a parametric study in [19]. Tighter waveguide spacing s leads to larger amounts of undesired guide-to-guide coupling. Transmitted power P_{in} is launched in each of these waveguides, with similar spectral distribution (driven by channelization, modulation rate, and modulation type). The energy coupled from one guide into the other can be treated as uncorrelated interference by virtue of their data streams being uncorrelated. The undesired coupled power will decrease the receiver signal-to-noise plus interference ratio (SINR), reducing data rates and potentially making detection and demodulation impossible.

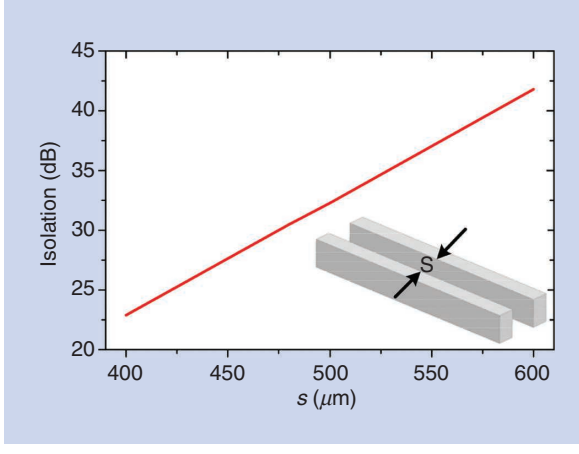

Figure 4. *The isolation between parallel rectangular dielectric guides, with guide-to-guide spacing s, in a notional terahertz interconnect system [19]. This plot assumes a 6-mm parallel geometry with identical guide cross sections and material. Each rectangular dielectric waveguide is modeled as a 300 × 500 μm² guide constructed from silicon and operating around 200 GHz.*

There are a number of strategies to ameliorate this effect if bandwidth density (i.e., bits per second per square millimeter) is a critical metric for the application, as is the case in many HPC and DC systems. For example, the use of higher dielectric constant waveguide material leads to tighter modal confinement and less guide-to-guide coupling. Another interesting strategy is to manufacture consecutive waveguides with slightly different propagation constants β for a designed operating mode. This so-called k-mismatch technique was pioneered in the integrated photonics community [29] to allow for smaller pitch between waveguides while

reducing guide-to-guide coupling. It was also studied from a theoretical perspective in [30], [31]. This mismatch can be achieved through a number of techniques, with the simplest being a choice of different guide cross-section dimensions or different materials with slightly different dielectric constants. Another approach utilizing orthogonal modes, from 90 to 120 GHz, has been studied in [28]. More recently, at higher frequencies, orthogonal modes were utilized in [17] to increase the usable bit rate in a rectangular dielectric waveguide.

Signal Sources

Historically, one of the most significant barriers to the use of terahertz waves for highly scaled computing applications has been the lack of efficient high-power sources in silicon processes. In the past, efficient generation of power in this regime at the milliwatt level was relegated to III–V sources and tended to be integrated with large waveguide assemblies for power transport. With increasing active device transition frequency f_T in integrated circuit technology, monolithic sources in the terahertz frequency range have begun to proliferate in the literature. Figure 5 shows a collection of recent power sources in the investigated frequency range. As one can see, there are a number of published results with milliwatt-class output powers in CMOS and silicon germanium (SiGe) processes in the 100–300-GHz regime. These technologies are of particular interest because they lend themselves to direct and large-scale integration with existing silicon design blocks. This provides a foundational capability to begin building progressively more complex and capable systems.

Wideband Terahertz Channelization

Similar to optical fiber interconnect and the use of wavelength-division multiplexing (WDM), the available single-mode bandwidths of these terahertz waveguides lends itself to the use of spectrally multiplexed data streams.

The use of novel and compact on-chip, on-interposer, or in-package filters can be considered for the implementation of physical broadband multiplexer devices. Careful performance and cost tradeoffs must be considered. Realization of high channel-count microwave multiplexers is challenging [33], [34], and components with finite quality factor lead to rigid bandwidth/loss tradeoffs.

Unfortunately, in the terahertz regime, on-chip and other planar structures suffer from the poor quality factor associated with conductor, dielectric, and radiative losses. Figure 6 shows an example of a compact folded quarter-wave resonator in the back-end metalization of a 130-nm IHP BiCMOS process. Using a high-frequency structure simulator (HFSS), the resonator's first-order eigenmode can be tuned between 220 and 330 GHz and realizes an unloaded quality factor (Q_u) of 20–30. This type of resonator is attractive because of the mixed electric and magnetic coupling, which can be realized via various arrangements and is relatively compact, allowing for the efficient realization of a higher-order filter [35]. Figure 7 shows an implementation and the full-wave simulated response of a terahertz triplexer in this back-end process. In this case, quasi-elliptical channel filter responses are designed in HFSS and star connected to form the overall channelizer response.

There have been a number of on-chip investigations of higher-Q structures, such as substrate integrated waveguide (SIW) filters in the terahertz regime [36]. These structures generally produce better Q resonators than transmission-line-based on-chip structures, but they are quite large. A number of different SIW geometries have been explored to reduce the structure's size, but they are limited by the process design rules and available metal layer thickness and spacing. In [37], a folded SIW was implemented in a

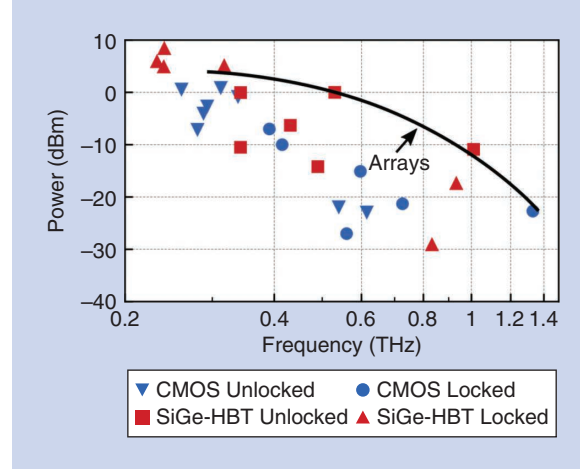

Figure 5. *A survey of contemporary terahertz sources in silicon from Pfeiffer's group at the University of Wupertal [32]. HBT: heterojunction bipolar transistor.*

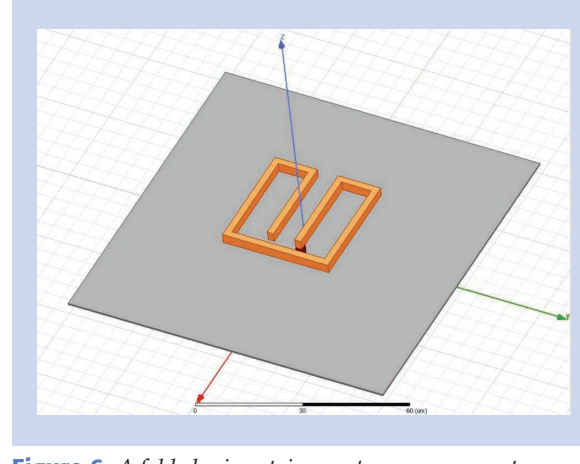

Figure 6. *A folded microstrip quarter-wave resonator, implemented in a 130-nm BiCMOS back-end-of-line processes provides simulated resonances from 220 to 330 GHz with Q_u from 20 to 30.*

130-nm CMOS process, realizing a 30% reduction in area for a transverse electric (TE10) mode waveguide.

Slow-wave structures have also been examined for the realization of on-chip terahertz filters. In [38], a V-band filter was realized in a CMOS back end, showing more than 30% size reduction over a conventional transmission-line-based approach. Once again, design rules and metal fill density requirements are significant drivers of overall performance and achievable resonator and filter geometries.

The losses associated with on-chip SIW structures arising from low aspect ratio and design rule considerations [36] tend to be higher than those realizable off chip. Indeed, conventional off-chip metallic waveguide-based approaches are well established and provide superior performance at these low power levels. A waveguide-based solution, however high performance, is still quite bulky at these frequencies, where wavelengths are on the order of a millimeter. The integration of such waveguide filters into an HPC or DC application is a nonstarter. Off-chip in-package filters may provide lower losses compared to their on-chip counterparts; however, they suffer from the relatively large manufacturing tolerances associated with semiconductor packaging processes. In [39], a 300-GHz transition from microstrip to a low-temperature cofired ceramic (LTCC) waveguide is demonstrated. Terahertz filters in LTCC have been successfully demonstrated in [40], [41]. Aside from single bandpass filters, SIW techniques have been successfully employed at lower frequencies to realize multiplexers [42]. Figure 8(a) shows one potential realization of an SIW-based triplexer in the terahertz regime. This manifold multiplexer is implemented in an interposer technology with integrated ground-signal-ground pads. This channelizer is designed for three channels: 220–250, 260–290, and 300–330 GHz. The current density is shown for the midband point for the highest channel. The resultant simulated wideband S-parameters are plotted in Figure 8(b). Stopband attenuation of 40 dB (or better) is achieved with fewer than 5 dB of midband insertion loss.

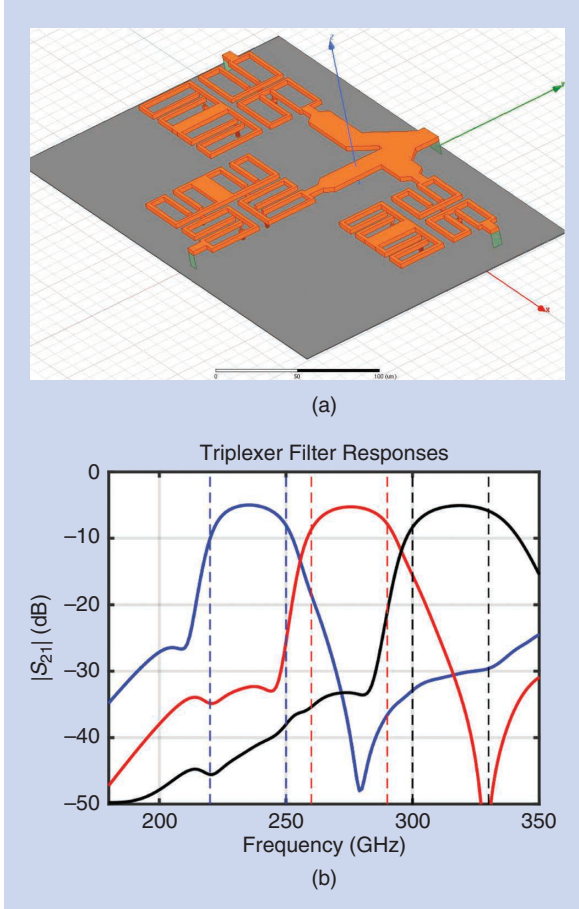

Figure 7. *The realization of a terahertz triplexer operating over 220–330 GHz, implemented in a silicon BiCMOS back end of line. (a) An HFSS model of a star-connected on-chip triplexer. (b) The full-wave simulation of the overall triplexer response, assuming 50-Ω source and load impedances. The dotted lines correspond to the design's desired channel filter bands.*

The tradeoffs associated with realizable resonator quality factor, required structural size, designed stopband attenuation, and so on all have direct impacts on the performance of a short-haul terahertz link. The "Link Budget Calculation" section discusses a number of design tradeoffs associated with this critical component in the context of an on-chip channelizer and their impact on overall link performance.

On-Chip Terahertz Power Couplers

The efficient coupling of power generated on chip into and out of the terahertz waveguide at the transmitter and receiver, respectively, is of critical importance. Unlike power couplers in the optical domain, where multiwavelength adiabatic tapers can achieve subdecibel coupling efficiencies, terahertz-regime power couplers are required to be subwavelength in size. Larger, more efficient coupling devices would require excessive chip or interposer area and become cost prohibitive or complicate integration.

As discussed in [5], on-chip power couplers at these frequencies have traditionally been forced into a number of design tradeoffs associated with bandwidth and efficiency. Moving the coupling structures themselves off chip alleviates this issue [Figure 9(a) and (b)], but it comes at the cost of additional loss to route the terahertz wave on/off chip as well as additional packaging complexity, itself tied to cost. Other approaches require the thinning of the high permittivity bulk silicon behind the coupling structure to reduce the undesired coupling of the modulated terahertz wave into bulk modes. This approach is also costly, requiring significant postprocessing. A third approach is the use of very high permittivity waveguide materials,

such as machined silicon [6], which has a number of advantages in terms of tight mode confinement [Figure 9(c)]. This lends itself to efficient coupling with low crosstalk between lanes, but the manufacturing required for large-scale integration is challenging. Additionally, significant challenges are associated with the packaging required to support a number of the existing schemes for physically interfacing the electromagnetic coupling structures with the waveguides themselves. These concepts are of the utmost importance when considering a scheme for large-scale integration into HPC, DC, and other planar applications (such as backplanes and so forth). Table 1 lists a number of different waveguide geometries, coupling approaches, and measured guide performance from a variety of sources above 100 GHz. The measured or estimated guide losses are normalized to 1 m, and the coupling losses listed are per coupler.

In [5], a broadband traveling wave structure is integrated in a BiCMOS back end of line to produce

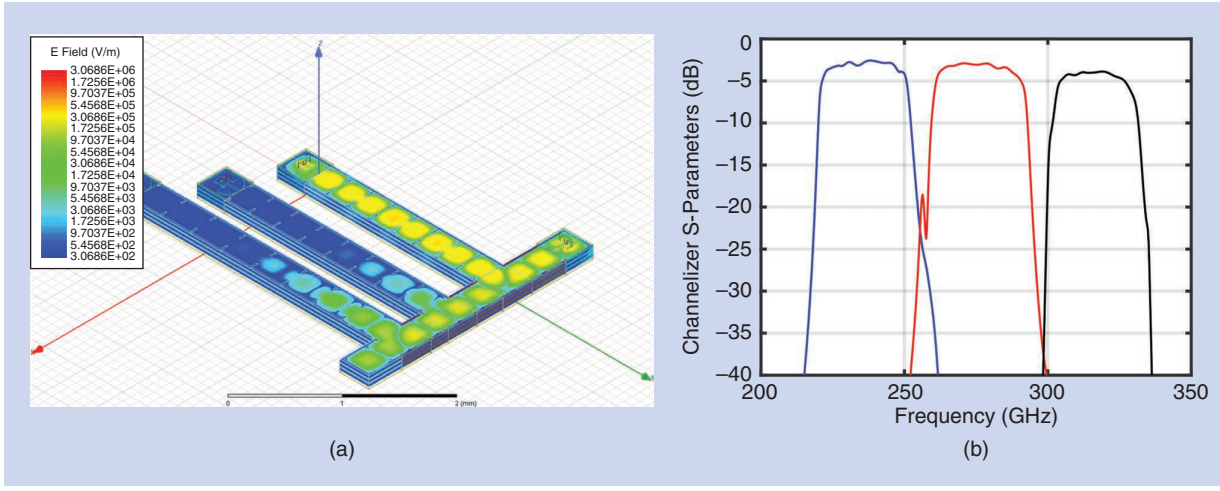

Figure 8. *A full-wave EM simulation of a triplexer utilizing an interposer technology. (a) The surface current density is shown at the middle of the top band: 315 GHz. (b) The triplexer transmission is shown from a broadband full-wave simulation.*

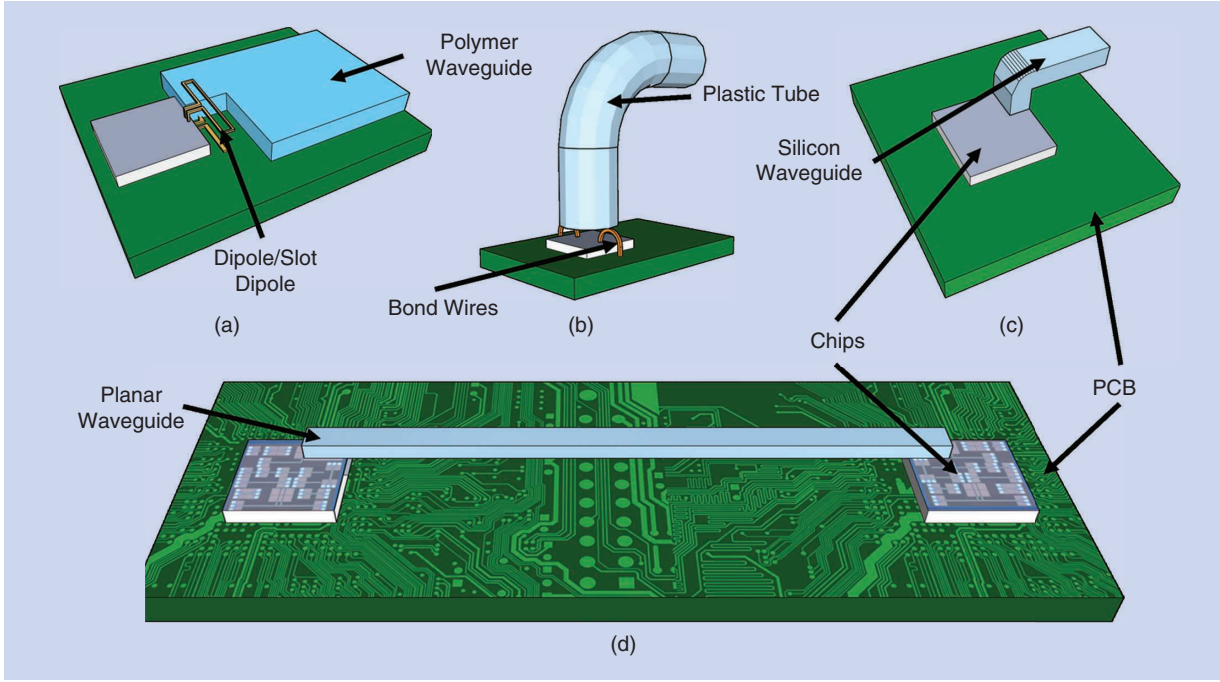

Figure 9. *Several concepts for the physical interface between a terahertz waveguide and the on-chip transceiver [5]. (a) An off-chip aperture excites the electromagnetic wave). In (b), the on-chip radiation inefficiencies are addressed through the use of bond-wire antennas, radiating into a circular waveguide. (c) A high-permittivity machined silicon waveguide and an on-chip aperture. (d) An on-chip aperture launching a broadband wave into a rectangular terahertz waveguide.*

broadband, low-loss coupling into a rectangular polymer waveguide [Figure 9(d)]. An example of the measured structures and waveguide placement, directly on the chip passivation layer, is shown in Figure 10(a). In this case, a coupling loss of fewer than 5 dB per coupler, after deembedding waveguide losses, was measured in H band [Figure 10(b)]. In addition, the transmission phase response, normalized to the waveguide length, is shown in Figure 10(c).

These integration concepts have a variety of system-level impacts, from waveguide and coupling losses to packaging considerations. Ultimately, tradeoffs associated with system cost, performance, and application will have to be made to determine the appropriate solution. For example, the use of entirely planar coupling geometries with rectangular waveguides might be considered for meter-class terahertz backplanes. Board-to-board interfaces may be better served via orthogonal coupling interfaces that utilize rectangular or circular waveguides. These choices will impact achievable lane data rates, data efficiency, lane-to-lane pitch (and associated aggregate data rates), and overall system cost.

Full-Link Demonstrations

With the proliferation of available couplers and waveguides as well as a variety of higher-frequency silicon sources and circuits, there have been several recent demonstrations of full end-to-end links (Table 2). These have focused on single-channel transmit/receive or full-duplex architectures. Independent channel aggregation has been demonstrated through the use of orthogonal guided modes. To date, we are unaware of any published integrated terahertz links making use of multiple-carrier RF channels aggregated and transmitted over a dielectric channel as depicted in Figure 2. However, the links that have been demonstrated push critical metrics, such as energy efficiency and realizable link lengths at terahertz frequencies. These demonstrations serve to show the tenability of the concept.

Terahertz Interconnect Architectural Tradeoffs

Canonical Architectural Concept

Given the large single-mode waveguide bandwidths available in the terahertz regime and the achievable operating bandwidths available in modern silicon nodes, a parallel channelization scheme is considered as a candidate for aggregate high-data-rate digital communication. Due to the large channel bandwidths and challenges associated with realizing gain at these frequencies in existing silicon processes, microwave multiplexers or channelizers are used to present constant impedances across the upconversion modulators' output bands. The channelizer ensures out-of-channel suppression and provides channel-to-channel isolation. This architecture also enables the choice of different modulation schemes, if appropriate, within each analog channel based on the channel's operating conditions. Various architectural tradeoffs can be made regarding the design and implementation of these channelizers. The "Link Budget Calculation" and "Aggregate Lane Data Rate and Energy-per-Bit" sections focus on the impacts of various channelizer performance parameters on overall lane capacity as well as link efficiency. In this example, we assume N channels, each with a 3-dB bandwidth of Δf within the total available transmission channel bandwidth BW_{WG} (Figure 11). The latter is determined by the transmission material properties, the modal characteristics of the waveguide, and the response of the structures used to couple energy between the waveguide and the on-chip structures and circuits.

Quantifying the performance of such a system can be achieved by examining a number of metrics, such as consumed energy per transmitted bit, aggregated across all of the channels on a given waveguide or lane. Other metrics of relevance include latency, a targeted bit error rate (BER), active area required to implement such a scheme, maximum achievable bit rate per lineal length,

TABLE 1. A survey of measured terahertz waveguide geometries and coupling schemes.

Reference	Frequency (GHz)	Guide Cross Section	Coupling Geometry	Guide Loss (dB*)	Coupling Loss (dB)
[5]	220–300	Rectangular	Planar on chip	50	4.8
[17]	130–210	Rectangular	Orthogonal off chip	40	6.5
[18]	90–220	Rectangular	Planar off chip	<100	2.2–3.3
[19]	210	Rectangular	Orthogonal on chip	100.6	3.6
[26]	60, 100	Rectangular	Metallic waveguide	8.7	—
[43]	100–600	Rectangular	Metallic waveguide	<2–19	—
[44]	140–190	Rectangular with taper	Planar off chip	14	0.44–1.5
[45]	80–100	Rectangular	Planar on chip	65.8	0.46
[46]	120	Round hollow	Orthogonal on chip	5.5	12

*The published results were normalized to a 1-m link to include losses from waveguide bends associated with the coupling geometry.

maximum achievable bit rate per waveguide cross-sectional area, or total cost per gigabit per second. Here, we concentrate on the energy per bit and aggregated data rate per waveguide required for this type of architecture given various component performance tradeoffs and current trends in silicon circuit performance.

Link Budget Calculation

Given the canonical multichannel architecture, we begin by modeling the available SNR at each channel receiver. In addition, due to the finite order of the multiplexer channel filters, we define the channel separation, consisting of guard bands of width δf, to ensure band-to-band isolation and ease of realization of the multiplexer design. Ideally, one would prefer to realize a channelizer that provides little insertion loss, has very high stopband attenuation, and minimizes the channel separation to provide the highest utilization of available aggregate waveguide bandwidth BW_{WG}.

To quantify the overall system-level performance tradeoffs associated with these parameters, we modeled the impacts of Δf, δf, and desired channel filter stopband attenuation As on the overall system performance, as it relates to total aggregate channel capacity and estimated energy per bit. To do this, we first consider a potential channel filter response: a type-II Chebyshev response because it provides excellent selectivity compared with other types of filter responses of a given order n and also provides a convenient set of closed-form expressions [50].

The design equations for estimating filter order based on these parameters is well known [51]. Utilizing an estimate of the filter order and the lumped filter prototype values (using [50]) and the assumed resonator Q_u, one can estimate the resultant channel filter insertion loss L_0 [52], [53].

Based on the H-band operating frequencies available in the polymer waveguide under investigation, midband insertion loss of a channel filter is a function of channel bandwidth Δf, desired stopband attenuation A_s, and channel separation δf. Utilizing a nominal Q_u of 20, based on an electromagnetic study of available subwavelength resonators realized in the back end of a commercially available 130-nm SiGe BiCMOS process (see the "Wideband Terahertz Channelization" section), the varying levels of passband insertion loss can be seen in Figure 12.

One can see that, given a specified Δf and A_s, changes in the channel separation δf have significant impacts on the insertion loss through each channel filter. This will necessarily impact available SNR at the receiver and thus impact that specific channel's available Shannon capacity:

$$C \propto \Delta f \cdot \log_2\left(1 + \frac{S}{N}\right). \tag{1}$$

Decreasing the channel separation provides a larger total aggregate number of channels and use of the available transmission bandwidth BW_{WG}, but, for a given filter order number n, this leads to an increase in channel filter loss or an undesired reduction in stopband attenuation for the same given passband insertion loss. This stopband attenuation is a concern because the adjacent channel energy is uncorrelated and will increase the in-band SINR and thus reduce the channel capacity. Increasing the order of the filter is one option, assuming the increase in stopband attenuation is much larger than the associated passband insertion loss, but one would strive to reduce the order of a given channel filter if cost or size constraints were a concern. Alternatively, one

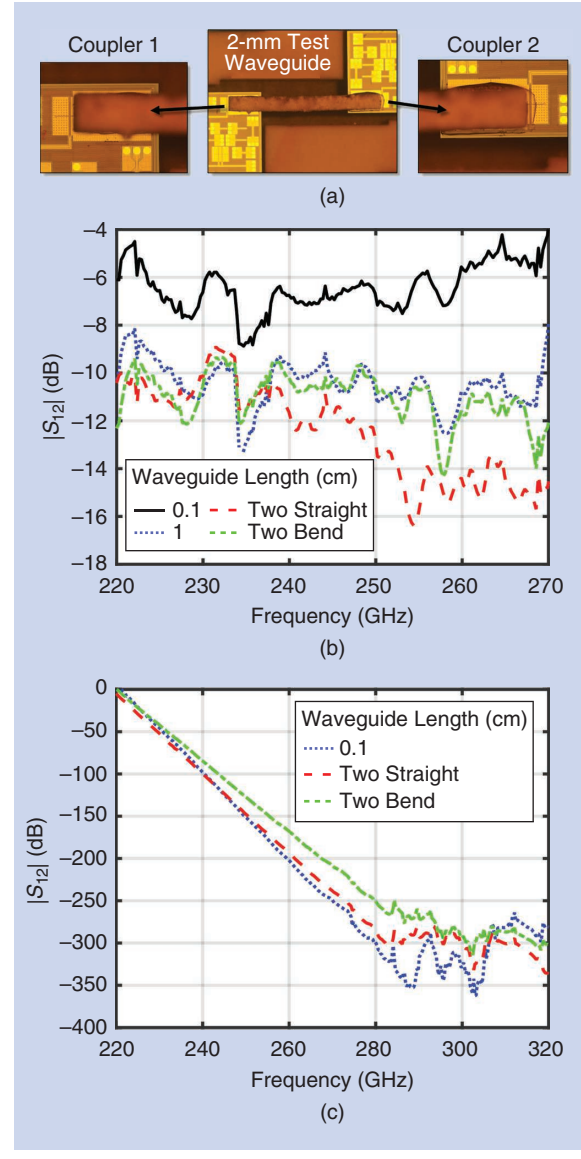

Figure 10. *(a) Photos of the chip and waveguide placement in which the rectangular dielectric waveguide is directly bonded to the chip passivation layer above the coupler structure, (b) the measured transmission magnitude, and (c) the phase response of a broadband on-chip terahertz power coupler and rectangular dielectric waveguide from [5].*

TABLE 2. The integrated terahertz links using dielectric waveguides.

Reference	Frequency (GHz)	Aggregate Data Rate (Gb/s)	Link Length (m)	Efficiency (pJ/b/m)	Notes
[46], [47]	120	12.7	1	1.8	
[48]	120	6.2	8	1.2	Full duplex
[49]	165	9.4	0.023	29.56	

might choose larger Δf channel sizes. This is an attractive solution, but a realistic implementation will suffer from the difficulty in realizing sufficiently wideband components capable of modulating, demodulating, and amplifying such large baseband bandwidths.

We select a nominal digital modulation scheme to help in analyzing these tradeoffs. In this case, we will carry out the following analysis utilizing a vestigial-sideband (VSB) binary phase-shift keying (BPSK) modulation. This scheme is chosen for its simplicity and the relative ease of transmitter realization at these sub-mm-wave frequencies as well the format's spectral efficiency.

For a given modulation rate

$$\frac{1}{T} = \Delta f$$

and a given transmitter power P, we make use of the modulated signal power spectral density

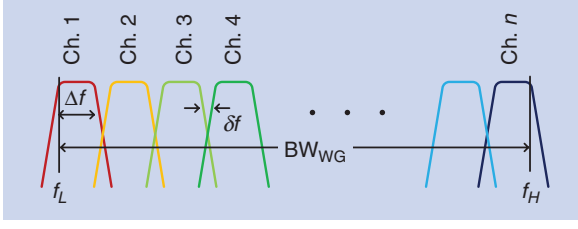

Figure 11. *The generalized channel structure on a single waveguide.*

$$S(f, f_{c,n}) = \frac{P \cdot T}{2}[\sin c^2((f - f_{c,n})T \cdot \pi) + \sin c^2((f + f_{c,n})T \cdot \pi)][\mathrm{W/Hz}] \quad (2)$$

at some carrier $f_{c,n}$ for each independent channel n. It should be noted that other modulation schemes can just as easily be used by the insertion of the appropriate $S(f, f_{c_n})$.

Figure 13 depicts a schematic of the spectral plan being analyzed in this article based on the link architecture of Figure 2. The parallel transmitter PSDs are shown, along with a representation of the idealized multiplexer response. The graph illustrates the impact of finite filter roll-off and stopband attenuation on in-band performance.

Assuming consistent modulation rates, modulation types, channel spacing, channel filter design specifications, and channel transmitter powers, using the PSD (2) we can estimate the in-band correlated signal power and the uncorrelated interference power from adjacent channels. A first-order approximation of the available desired signal power in the nth passband can be written as

$$P_{\mathrm{signal}} \approx 10^{-L_{pb}/10} \int_{f_{c,n}}^{f_{c,n}+\Delta f} S(f, f_{c,n})\, df\,[\mathrm{W}],$$

for the total loss in the passband through the multiplexer and channel as

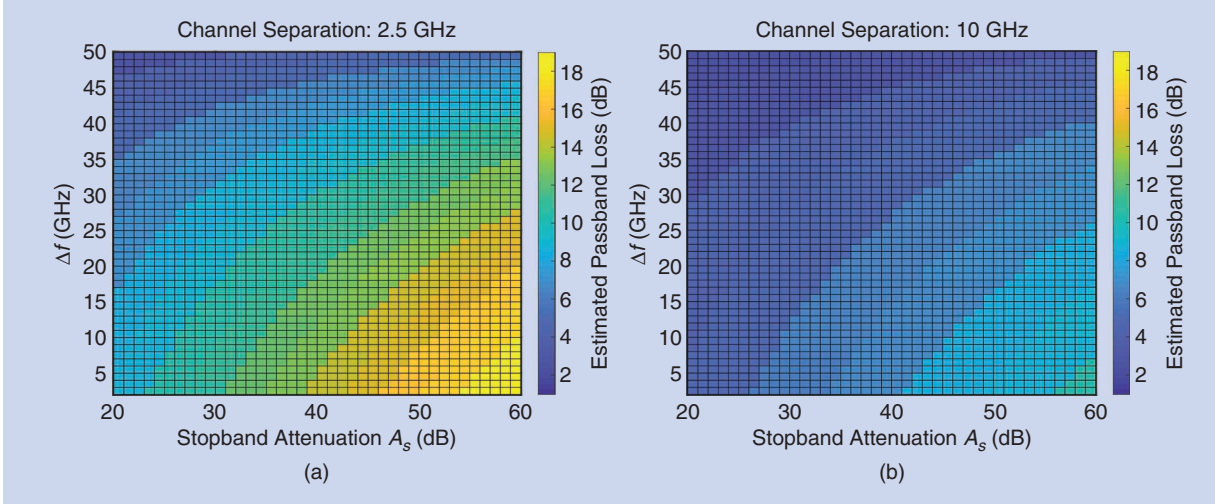

Figure 12. *The estimated passband insertion loss for two different channel separations; (a) δf = 2.5 GHz and (b) δf = 10 GHz.*

$$L_{pb} = 2A_P + L_{ch}\,[\text{dB}],$$

with the coupler and channel loss combined in

$$L_{ch} = 2L_{cpl} + L_{WG}\,[\text{dB}].$$

Similarly, we approximate the uncorrelated interference power from the $(n-1)$ lower band present in the band of interest as

$$P_{\text{int}LB} \approx 10^{-L_{sb}/10} \int_{f_{c,n-1}+\Delta f+\delta f}^{f_{c,n-1}+2\Delta f+\delta f} S(f, f_{c,n-1})\,df\,[\text{W}],$$

with the out-of-band attenuation (assuming a symmetric channel filter response) of

$$L_{sb} = A_s + A_P + L_{ch}\,[\text{dB}].$$

Last, we account for the undesired lower or VSB energy present in the nth band of interest from the $(n+1)$-th band as

$$P_{\text{int}UB} \approx 10^{-L_{sb}/10} \int_{f_{c,n+1}+\delta f}^{f_{c,n+1}+\Delta f+\delta f} S(f, f_{c,n+1})\,df\,[\text{W}].$$

We note that no special treatment is given to the first and last channels; they will encounter less undesired out-of-band interference energy. This improvement in the signal-to-interference level is not modeled. As a result, we expect the link performance to be slightly better, in aggregate, than this model predicts. The total interference in the nth band can be approximated as

$$P_{\text{int}} \approx P_{\text{int}UP} + P_{\text{int}LB}\,[\text{W}].$$

In addition, the individual receiver implementation will exhibit a noise floor

$$P_{N-rx} = -204\ \text{dBW/Hz} + 10 \cdot \log_{10}\Delta f + NF_{rx}\,[\text{dBW}]$$

due to the noise equivalent bandwidth and the receiver finite noise figure NF_{rx}. The signal-to-noise plus interference is written as

$$\text{SINR} = \frac{P_{\text{signal}}}{P_{\text{int}} + P_{N-rx}}. \tag{3}$$

Equation (3) can be used to perform a parametric analysis on the SINR impact of various channel filter performance metrics and guard-band spacings. Similarly, this type of system-level model can used with any other type of modulation through a simple substitution for the appropriate PSD $S(f)$.

Figure 14 shows the estimated SINR as parameterized over various values of A_s, Δf, and δf of a single channel, given a 1-mW source that encounters 10 dB of conversion loss through the terahertz modulators. The loss associated with the wideband coupler is 5 dB [5]. We assume 5 dB of total loss in the waveguide medium. The receiver performance is modeled with a 20-dB noise figure and a 10-dB conversion loss.

One can see that the SINR improves, in general, for a given channel bandwidth Δf as the stopband attenuation increases. Similarly, we see that larger channel-to-channel spacing also improves the channel SINR, but this comes at the cost of unused spectrum on a given waveguide. Similarly, an increase in the stopband attenuation for a given δf and Δf is associated with an increase in the filter order, size, and cost. This growth in filter size could potentially limit the available number of lanes one could implement on a given area. Note that the size of the resonators is on the order of the carrier wavelength (around 1 mm at these frequencies), and their number is proportional to filter order n.

Given the energy outside of the first Nyquist band for this type of modulation (Figure 11), the idealized flat stopband response, and the large equivalent noise bandwidth contribution to the overall receiver noise floor, we expect the noise floor to be dominated by the channel-equivalent noise bandwidth. Given other types of modulation, other filter implementations, or even changes in available component quality factor, these trends can change.

Aggregate Lane Data Rate and Energy-per-Bit

Our ultimate goal is maximizing the bandwidth density for a given waveguide, while minimizing the energy required to modulate, transport, and demodulate the data. We build upon the SINR analysis presented in the previous section and illustrated in Figure 14. For a given available lane bandwidth BW_{WG}, channel-to-channel guard bandwidth δf, and channel bandwidth Δf, the number of available channels per lane is

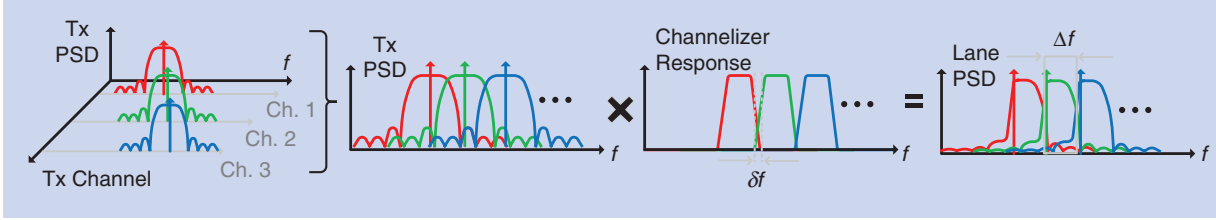

Figure 13. *The VSB terahertz interconnect spectral plan being analyzed. Parallel double-sideband BPSK modulation occurs across N channels, undergoes filtering (via multiplexer channel filters) to suppress the modulated lower sideband, and multiplexes independent channels onto a single waveguide.*

$$N = \left\lfloor \frac{BW_{WG} + \delta f}{\Delta f + \delta f} \right\rfloor.$$

Given the available channel capacity (1), number of channels per lane N, and the channel SINR (3), we can calculate the total aggregate lane capacity as

$$C_{WG} \propto N \cdot \Delta f \cdot \log_2(1 + \text{SINR}), \tag{4}$$

presented in Figure 15. In this analysis, one might select an architecture that maximizes the available channel bandwidth Δf, utilizing a diplexer to provide the channelization with large stopband attenuation. There is little published work on monolithically integrated silicon-based modulators capable of achieving those types of modulation bandwidths (>50 GHz) in the G or H bands (140–330 GHz). In addition, selecting smaller channel separation [Figure 15(a)] requires a more stringent out-of-band channel filter attenuation to reduce the in-band SINR. As discussed previously, this leads to an increase in system complexity, size, and cost.

Furthermore, scaling the baseband rate Δf comes with a commensurate increase in the power requirements for a variety of baseband components (amplifiers and so forth). This bandwidth–power tradeoff in transmitter modulator and baseband circuitry is not included in this analysis. Given analytical models, one would see a diminishing advantage as the channel bandwidth increases. Similarly, the impacts of dispersion related to both the lane waveguide as well as the multiplexer filter shape and order, the subsequent equalization requirements, and the related power overhead are also not modeled here.

We again consider the specific case of the VSB BPSK modulation described in the "Link Budget Calculation"

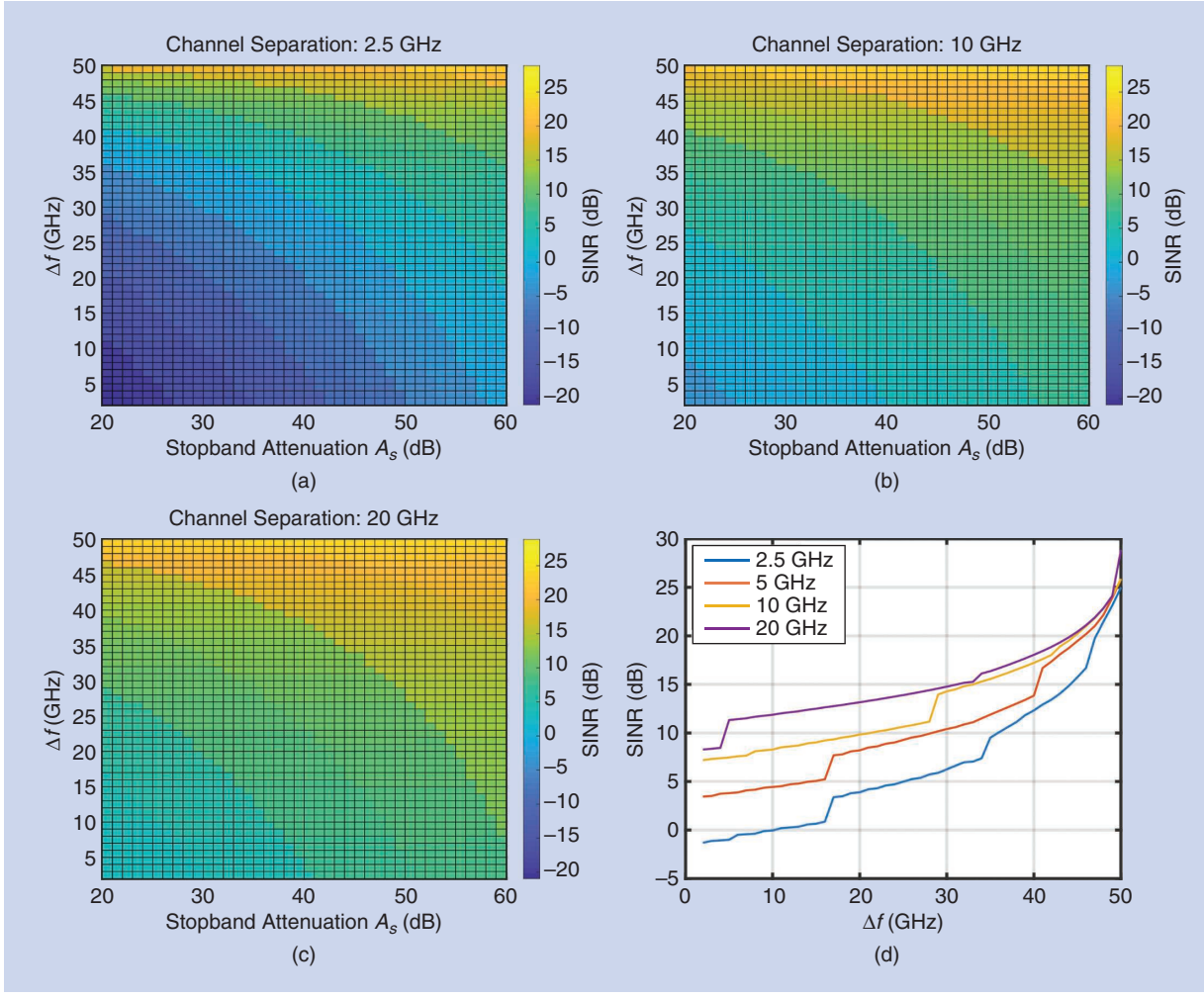

Figure 14. *The SINR estimates versus channel bandwidth and channel filter stopband attenuation for a VSB BPSK-modulated terahertz carrier with (a) 2.5-GHz, (b) 10-GHz, and (c) 20-GHz channel–channel separation. (d) The best SINR estimate available for a given Δf for a variety of δf values. The discontinuities in (d) are associated with steps in the filter order n required to meet a given A_s specification.*

section and impose a specific BER requirement. The channel capacity can then be defined as previously for a given SINR to provide that required BER. For the case of a 10-GHz channel separation, the aggregate channel capacity, given BPSK modulation, is shown in Figure 16(a). Given this modulation, the modeled achievable lane capacity, assuming a minimum SINR, is primarily defined by the available channel bandwidth. Therefore, we expect relatively flat capacity dependence on the channel bandwidth Δf. In Figure 16(a), the discrete steps corresponding to changes in lane capacity are due to changes in required filter order to meet the given fractional bandwidth requirements of a given Δf. The BER figures, however, are strongly tied to the in-channel SINR figures. One can see the relationship between an increase in designed stopband attenuation at a given channel bandwidth and the subsequent improvement in BER. In this case, realizable on-chip or interposer-based multiplexers might drive one to stopband attenuation specifications on the order of 40 dB. In this case, to meet the given BER rate, one would choose channel bandwidths on the order of 30 GHz to maximize the available aggregate lane data rate.

Recall that we are concerned with not only aggregate data rate per lane but also the energy per bit required to transmit and receive the data. Assuming a 2.5% dc–RF efficiency for baseband circuitry, carrier generation, modulation, and down-conversion (carrier generation being the largest contributor to overall link efficiency), we can estimate the energy per bit [Figure 16(b)] for the maximum throughput case (assuming Shannon capacity). In this case, as well, one can see that the optimal energy per bit occurs at $\Delta f \approx 30$ GHz with around 40 dB of stopband attenuation.

Full-Link Simulation Results

Utilizing the analysis of the notional architecture in Figure 2 discussed in the "Terahertz Interconnect

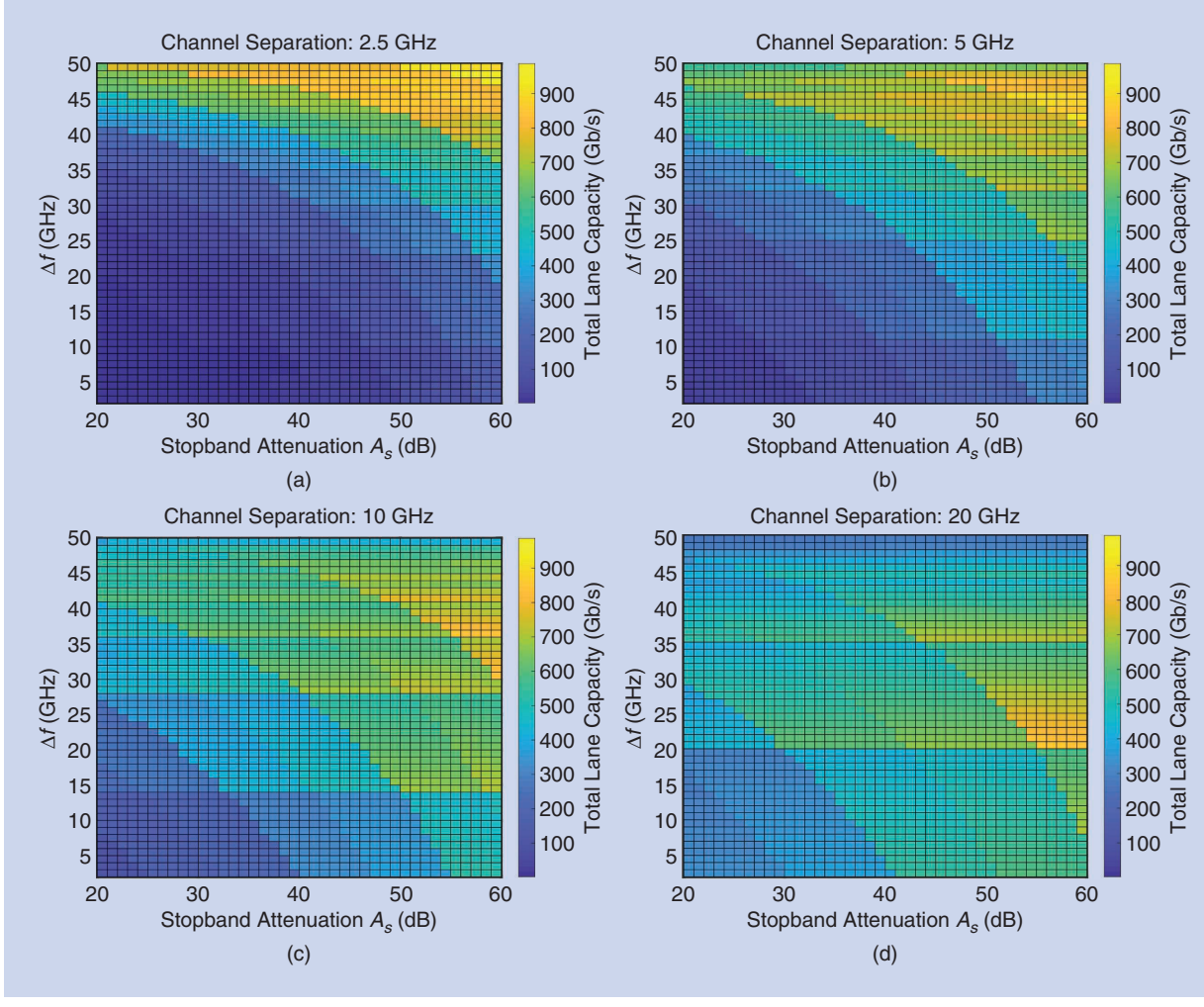

Figure 15. *The aggregate Shannon channel capacity per waveguide for (a) 2.5-GHz, (b) 5-GHz, (c) 10-GHz, and (d) 20-GHz channel spacing. This analysis assumes $BW_{WG} = 110$ GHz of contiguous, single-mode waveguide bandwidth. Some higher-order modulation schemes are assumed to approach the channel Shannon capacity, with total system dc–RF efficiency of 2.5%.*

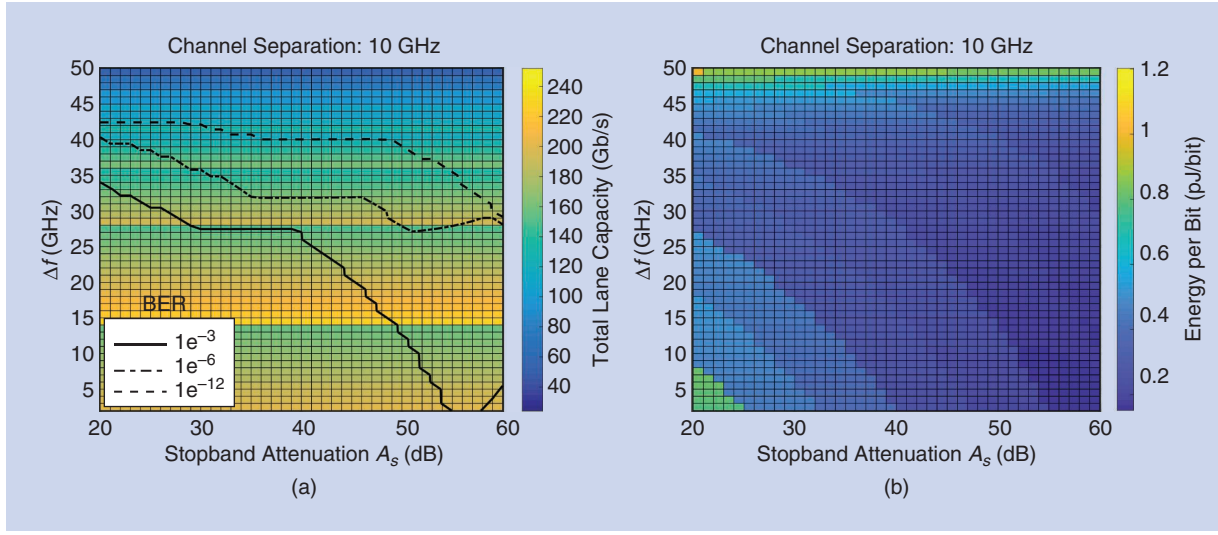

Figure 16. *(a) The aggregate lane channel capacity for a VSB BPSK-modulated set of carriers with a 10-GHz channel separation. The three constant-BER contours correspond to BERs of 10^{-3}, 10^{-6}, and 10^{-12} (the bottom, middle, and top contours, respectively). Regions above these contours provide sufficient SINR to achieve BERs better than these values. Regions below these lines will generate higher BERs. In this case, a 5% dc–RF efficiency is assumed due to the simple nature of the modulation scheme. (b) The estimated energy per bit (Shannon capacity) with a 10-GHz channel separation. This estimate assumes high-order modulation; with the added complexity, a 2.5% dc–RF efficiency is assumed.*

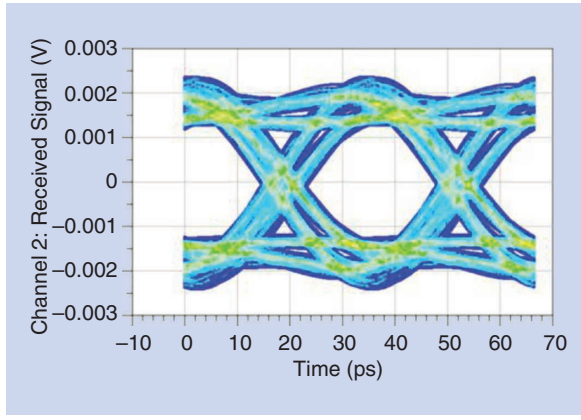

Figure 17. *A simulated eye diagram of a 90-Gb/s aggregate rate lane, carried over a terahertz waveguide. The baseband received voltage from a PRBS bitstream for channel 2 (260–290 GHz) is shown.*

Architectural Tradeoffs" section, a simulation was carried out to verify the previous analysis. A 10-cm rectangular dielectric waveguide made from Rogers R3003 PCB material and utilizing a broadband power coupler based on the work in [5] was employed for the channel. A three-channel architecture was chosen with Δf =30-GHz channel bandwidths and δf = 10-GHz guard bands. A coherent VSB modulation scheme was utilized with baseband raised-root cosine intersymbol interference filtering. Electromagnetic (EM)-circuit models (based on a commercially available BiCMOS technology) of subharmonic mixers were used for phase modulation and heterodyne detection. Similarly, baseband circuitry and local oscillator generation were simulated using EM-circuit models. The individual transmit chains were driven with independent (uncorrelated) 30-Gb/s pseudorandom bit sequences (PRBSs) of length 2^{15}. The simulation makes no use of additional receiver baseband amplification. In addition, the simulation utilizes neither baseband preemphasis nor receiver equalization. Cursory examination shows eye-opening improvements with the use of simple single-tap baseband preemphasis or analog feed-forward equalization. As can be seen in Figure 17, the eye opening is sufficient to close the link without the use of additional equalization techniques at an aggregate lane rate of 90 Gb/s over the three independent channels. The middle channel, which one expects to be the most susceptible to interference from adjacent channel interference, is shown in the plot. Without equalization, eye openings larger than 2 mV can be seen.

Conclusions

Review of Terahertz Interconnect Tradeoffs

It should be noted that this analysis is highly dependent on a number of application-specific factors and design choices. First, the waveguide (or channel) losses are largely a function of material properties and waveguide geometry. Cost, manufacturability, integration scheme, guide-to-guide coupling, and chromatic dispersion should all be considered. These considerations will drive the link attenuation as well as provide a

maximum for a given channel's signaling rate at a specific link length. In addition, guide-to-guide coupling will drive the maximum achievable bandwidth density at a given link length.

Once the waveguide configuration is chosen, a coupler that is capable of supporting the operating frequency and bandwidths of interest will have to trade off area (cost), ease of integration, efficiency, and bandwidth against each other. The performance of the waveguide and coupler will establish a baseline level of link loss, L_{ch}. Similar to fiber-optic interconnects, the loss mechanisms in these types of terahertz interconnects will exhibit fairly flat attenuation characteristics across the applicable link length scales [4].

As a result, focus should then shift to the terahertz channelization, carrier frequency generation, and modulation as well as baseband circuitry. Again, the overall link efficiency will largely depend on the efficiency of these components. As was discussed in the "Link Budget Calculation" section, the choice of on- or off-chip multiplexers will have significant impacts on achievable spectral performance. This will, in turn, have substantive impacts on the overall link performance.

Areas of Future Investigation

Following the survey of prior work in all of the constituent components in the "Enabling Technologies" section, it is clear that there are various areas where continued exploration will provide significant improvements in performance and cost associated with the implementation of these types of links.

The continued development and characterization of materials for use as terahertz guides are important. This will, in turn, inform the achievable performance for a variety of different types of guide geometries—beyond the simple rectangular dielectric waveguide presented here. Taking cues from the integrated photonics community may prove useful in increasing achievable lane densities in the context of longer interconnects that might be found in board-to-board applications.

The solid-state circuits community has pursued, and continues to aggressively pursue, increased terahertz signal source power and efficiency. They continue to leverage device feature scaling—and, more importantly, device speed scaling. A focus on lowering phase noise will become more important as this type of interconnect becomes a more feasible alternative to higher-loss electrical copper-based interconnects or more expensive optical interconnects. In addition, the circuit community continues to pursue increasing signaling rates and efficiencies in baseband circuitry to address optical interconnect/communication. Terahertz interconnect technologies can directly leverage these efforts toward more efficient baseband technologies.

The use of multiple parallel transceivers, just as in optical WDM schemes, requires continued work on efficient and high-performance channelization/multiplexing schemes. There is a wealth of information and experience in this area as it relates to the software-defined radio community for access to lower-frequency bands and smaller bandwidths. This is an area where research could contribute substantially to improve the overall receiver SINR—and thus lead to improvements in channel and lane rates as well as potentially significant improvements on lane efficiency.

Realizing high-performance analog multiplexers will be important to the successful demonstration of these types of links. The choice of on- or off-chip multiplexer has a number of packaging, cost, and performance implications. These implications require codesign of the associated transceiver circuitry, the wideband power coupler, and the waveguide itself.

Last, the development of efficient and broadband power couplers for terahertz interconnects is another area for further work. The choice of waveguide/package/coupler integration concept, waveguide material, waveguide geometry, and operating bandwidth and the decision to utilize on- or off-chip coupling structures all play pivotal roles in realizable performance. This is a rich area in which a number of new and different concepts could be pursued. Achieving subdecibel coupling loss would contribute almost an order of magnitude improvement in current state-of-the-art SINR and efficiency figures in these types of links. Just as in the multiplexers, this would have significant impacts on lane rates and efficiency. The use of new topologies and materials in multichip module or system-in-package technologies is interesting and may provide an attractive path forward.

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