A Terahertz Molecular Clock on CMOS Using High-Harmonic-Order Interrogation of Rotational Transition for Medium/Long-Term Stability Enhancement

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Abstract—Chip-scale molecular clocks (CSMCs) perform frequency stabilization by referencing to the rotational spectra of polar gaseous molecules. With potentially the “atomic” clock grade stability, cm-level volume and <100 mW DC power, CSMCs are highly-attractive for the synchronization of high-speed radio access network (RAN), precise positioning and distributed array sensing. However, the medium/long-term stability of CSMCs is hindered by the transmission baseline tilting due to the uneven frequency response of the spectroscopic system and the molecular cell. To enhance the medium/long-term stability, this paper presents a CSMC architecture locking to the high-odd-order dispersion curve of the 231.061 GHz rotational spectral line of carbonyl sulfide (OCS) molecules, which is selected as the clock reference. A monolithic THz transceiver generates high-precision, wavelength-modulated probing signal. Then, the wave-molecule interaction inside the molecular cell translates the frequency error between the probing signal and the spectral line center to the periodic intensity fluctuation. Finally, the CSMC locks to the 33rd-order dispersion curve after a phase-sensitive lock-in detection. In addition, a pair of slot array couplers is employed as an effective chip-to-molecular cell interface. It leads to not only a higher SNR, but also a significantly simplified CSMC package. Implemented on a 65 nm CMOS process, the high-order CSMC presents a measured Allan deviation of 4.3×10−11 under an averaging time of $\tau = 10^3$ s, while consuming 70.4 mW DC power.

Index Terms—chip-scale molecular clock, rotational spectroscopy, OCS, Allan deviation, CMOS, frequency stability, high order dispersion curve

I. INTRODUCTION

HIGHLY stable, miniaturized, power efficient and low cost clocks are increasingly important for the emerging electronics. For instance, augmented/virtual reality (AR/VR) devices, real-time multi-person online gaming and autonomous driving all require radio access networks (RAN) with high capacity ($\sim$1 Gbit/s throughput per node), high density (1-million nodes per km$^2$) and low latency (1~10 ms) [1], [2]. It leads to the stringent requirements for clock synchronization. For example, the international telecommunication union (ITU) specifies a maximum relative timing error of 65 ns for the massive multi-input-multi-output (MIMO) systems of 5G new radio (NR) [3]. Furthermore, the positioning service through 5G base stations demands a 10-ns relative timing error for a 3-m accuracy [1]. However, only a $\mu$s-level timing accuracy has been provided for the current 4G-LTE base stations relying on the precision timing protocol (PTP) with the global positioning system (GPS) [4]. On top of that, it is worth mentioning that the GPS accuracy degradation and signal blockage commonly occur in urban areas and indoor environments, where 5G NR base stations are to be deployed [5]. In addition, the cost of synchronization networks is also critical. On one hand, compact 5G base stations are heavily densified due to the high data throughput and the limited signal coverage [6]; on the other hand, a significant cost reduction per unit bandwidth at the user end is expected. The usage of traditional atomic clocks, which are bulky and expensive, as the backbone of synchronization networks becomes problematic [7], calling for new high-stability clocks with low cost and small size. Another potential application of these clocks is the ocean bottom seismographs for oil exploration [8]–[10]. The massive acoustic sensor networks reconstruct the geometric structure beneath the ocean floor according to the precise arrival time of the reflected sonic pulses. The acoustic sensors experience tens of celsius of temperature variation while sinking to the ocean floor. Meanwhile, powered by batteries, they stay under a GPS-denial environment for up to a year. To keep the required timing accuracy of 1~10 ms over this period, the sensor clock should provide a stability at 10$^{-11}$ level, while keeping its power low.

Existing technologies do not completely fulfill the current needs. The widely-adopted oven compensated crystal oscillators (OCXO) [11], [12] and MEMS oscillators (OCMO) [13]–[15] isolate the resonators from the surrounding environment using a heated oven. The clock frequency is further regulated by the temperature compensation [16], [17]. The OCXO/OCMO provide decent temperature stability of 10$^{-7}$ $\sim$ 10$^{-8}$ over the full temperature range (-20°C~+70°C) [11], [12]. However, their DC power is at watt level in steady-state, and is even higher during start-up. Alternatively, chip-scale atomic clocks have been developed [18]–[20]. They are referenced to the electronic transitions of Alkali atoms (e.g. Rubidium (85Rb) or Caesium (133Cs)). The utility of coherent population trapping (CPT) [21] and micro-fabricated vapor cell [22] enables significant miniaturization and power reduction.
The CSAC in [23] achieves a stability of $\pm 1 \times 10^{-9}$ within $-10^\circ C$ to $+70^\circ C$, while only consuming 60-mW DC power. However, the CSACs possess several disadvantages: (1) A high cost due to sophisticated optical-electrical construction. The required vertical cavity surface emitting laser (VCSEL) with precise 894.6 nm (D1) or 852.3 nm (D2) laser wavelength for $^{153}$Cs atom probing has low yield [24]. Advanced MEMS and packaging technologies are applied for the tight integration of VCSEL, laser detector, micro-fabricated vapor cell and microwave circuitry. (2) Susceptibility to external magnetic fields due to the strong magnetic dipole of electron spins. As a result, all CSACs are equipped with a magnetic shield to alleviate the problem [25]. (3) A slow start-up procedure. After a cold start, the clock package should be heated to around 80°C for Alkali metal evaporation, and then temperature-stabilized with mK-level accuracy to ensure precise laser wavelength. For instance, the Microsemi SA.45s CSAC needs 3 minutes for its start-up procedure [26].

Recently, the rotational spectra of polar gaseous molecules in the terahertz range emerge as new physical references for clock stabilization [27]. A rotational spectral line could have a high quality factor ($\sim 10^6$) and strong absorption intensity. Meanwhile, THz spectrometers on CMOS have been demonstrated [28]–[32]. Thus, low-cost clocks at chip scale and with “atomic” clock grade stability become possible. The first chip-scale molecular clock (CSMC) chipset on 65 nm CMOS locks to the 231.061 GHz rotational spectral line of carbonyl sulfide ($^{16}$O$^{12}$C$^{32}$S) molecules in gas phase [33], [34]. It presents an Allan deviation of $\sigma_y = 3.8 \times 10^{-10}$ with an averaging time $\tau = 10^3$ s and a 66 mW DC power. It enables a fast start-up, and all-electronic configuration potentially leading to dramatic cost reduction compared with CSACs. However, its medium/long-term stability with the presence of temperature fluctuation is degraded by the tilting of its spectroscopic transmission baseline. Such tilting is caused by the inevitable, uneven frequency response of the THz spectrometer and the molecular cell. In Section II, we show that it leads to a spectral line profile with a temperature-dependent asymmetry, which cannot be corrected by the 1st-order dispersion curve probing approach adopted by the CSMC [34], [35].

In this paper, a new CSMC locking to a high-odd-order dispersion curve is demonstrated [36]. It also references to the 231.061 GHz spectral line of OCS molecules. By performing a 3rd-order derivative on the asymmetric line profile, the new dispersion curve generated by the clock exhibits less temperature dependency and thus, the medium/long-term stability of the clock is significantly improved. In this 65-nm CMOS chip, a high-order spectroscopic system is implemented with enhanced sensitivity and signal purity. In the experiments, the CSMC achieves Allan deviations of $\sigma_y = 3.2 \times 10^{-10}$ @ $\tau = 1$ s and $\sigma_y = 4.3 \times 10^{-11}$ @ $\tau = 10^3$ s. Compared to the prior CSMC [34], [35], an ~8x stability improvement is obtained with a similar DC power of 70.4 mW. In addition, a single-chip realization is achieved through employing a pair of slot array couplers as an effective chip-to-molecular cell interface. It results in further packaging simplification and cost reduction. This paper is organized as follows: in Section II, the impacts of transmission baseline tilting and the high-order molecular probing scheme are illustrated. In Section III, the architecture of CSMC enabling the probing scheme is presented. Section IV discusses the details of the circuit blocks. Then, Section V presents the clock packaging and the experiment results. Section VI concludes this paper with a comparison with the other state-of-the-art time-keeping devices.

II. TRANSMISSION BASELINE TILTING AND HIGH-ODD-ORDER DISPERSION CURVES

A simplified schematic of CSMCs is shown in Fig. 1a. A wavelength modulated THz probing signal $V_{WM}(t)$ is generated by a THz transmitter (Tx) referenced to a voltage-controlled crystal oscillator (VCXO). The VCXO determines the short-term clock stability (Fig. 1b). The instantaneous frequency $f_p(t)$ (Fig. 2a) of $V_{WM}(t)$ is expressed as:

$$f_p(t) = f_m + \Delta f \sin(2\pi f_m t),$$

where $f_p$ is the center frequency, $f_m$ is the modulation frequency, and $\Delta f$ is the frequency deviation. The gas absorption coefficient $\alpha(f)$ of the selected spectral line has a Lorentzian profile due to the pressure broadening [37], [38], which can be decomposed into a complex form as follows:
The mathematical derivatives of the Lorentz profile and the simulated odd-order dispersion curves with $\Delta f = 100$ kHz and 1 MHz, respectively. $f_m=0.1 \times \Delta f$. The amplitude is normalized. The polarization is aligned for a better comparison.

\[
\alpha(f) = \frac{f_p^2}{f_h^2 + (f - f_0)^2} = \beta \left[ \frac{1}{f_h + (f - f_0)i} + \frac{1}{f_h - (f - f_0)i} \right],
\]

where $\alpha_p$ is the peak absorption coefficient in the spectral line center $f_0$, $f_h$ is the half width at half maximum of a specific spectral line, and the coefficient $\beta = \alpha_p f_h/2$. After the wave-molecule interaction, the intensity of the probing signal is periodically modulated as shown in Fig. 2a. Then, a THz square-law detector (Fig. 1) converts the intensity fluctuation into the baseband signal $I(t)$:

\[
I(t) = I_0 \cdot e^{-\alpha(f_p(t))L} \approx I_0 \cdot (1 - \alpha(f_p + \Delta f \sin(2\pi f_m t))L),
\]

where $I_0$ is the baseband signal without the gas absorption, $L$ refers to the path length of the molecular cell. $\alpha(f)L \ll 1$ is assumed in (3). Note that $I(t)$ has abundant harmonics of $f_m$. Correspondingly, (3) can be decomposed as:

\[
I(t) \approx I_0 \left[ 1 - \sum_{n=0}^{\infty} V_{LKN}(f_p) \cos(2\pi N f_m t) \right],
\]

where $V_{LKN}(f_p)$ is the $N^{th}$ Fourier component of the baseband signal at $f_p$, $N \in \{1, 2, \ldots \infty \}$. By assuming $\Delta f \ll f_{WHM}$, where $f_{WHM}=2f_h$ is the full width at half maximum of the spectral line, $V_{LKN}(f_p)$ can be expressed as [39], [40]:

\[
V_{LKN}(f_p) \propto L \frac{a_{LKN}^{1-N} \Delta f_m}{N!} \frac{d^N \alpha(f)}{df^N} \bigg|_{f=f_p}.
\]

$V_{LKN}(f_p)$ is proportional to the $N^{th}$-order derivative of $\alpha(f)$ in (5). In Fig. 1a, with the switch $K$ “open”, $V_{LKN}(f_p)$ is measured by a phase-sensitive lock-in detector. By sweeping $f_p$, $V_{LKN}(f_p)$ can be recorded as the $N^{th}$-order dispersion curve (Fig. 2b). The $N^{th}$ order derivative of the gas absorption coefficient $\alpha(f)$ in (2) can be expressed as:

\[
\frac{d^N \alpha(f)}{df^N} \bigg|_{f=f_p} = N! \cdot \beta \cdot \left[ \frac{(-1)^N}{(f_h + (f - f_0)i)^{N+1}} + \frac{1}{(f_h - (f - f_0)i)^{N+1}} \right].
\]

While the center frequency of probing signal coincides with the spectral line center $f_p = f_0$, (6) can be written as:

\[
\frac{d^N \alpha(f)}{df^N} \bigg|_{f=f_p=f_0} = N! \cdot \beta \cdot \frac{(-1)^N + 1}{f_h^{N+1}}.
\]

As a result, while $f_p = f_0$, all of the odd order derivatives equal 0. Accordingly, (5) indicates that the baseband signal...
$I(t)$ only has even order harmonics of $f_m$, which is shown in Fig. 2a. Since $V_{L,K,N}(f_p)$ is 0 for all of the odd order harmonics, the odd-order dispersion curves exhibit a zero-crossing point at $f_p=f_0$ (Fig. 2b), which provides the amplitude and polarization of frequency feedback control. Hence, the odd order dispersion curves can be adopted in CSMCs [27]. With a small frequency deviation (e.g. $\Delta f=100$ kHz $\ll f_{FWHM}=1.47$ MHz [34] in Fig. 2b), the dispersion curves match well with the mathematical $N^{th}$-order derivative of the spectral line profile. However, a large $\Delta f$ is generally used for a higher loop gain and SNR. As shown in Fig. 2b, the dispersion curves deviate from the math with $\Delta f=1$ MHz. For more details on wavelength modulation spectroscopy (WMS) with a large $\Delta f$, Wahlquist [41] and Arndt [42] gave thorough analyses. Then, by “closing” the switch $K$ in Fig. 1a, the CSMC locks to the zero-crossing point $f_p=f_0$ of the selected odd-order dispersion curve. After the locking, the clock stability in the medium-term is inversely proportional to the $Q\times$SNR product [27] (Fig. 1b), where $Q$ refers to the quality factor of the spectral line. With a fixed $Q$, a CSMC with higher SNR presents better medium term stability.

Fig. 1b reveals that the clock medium/long-term stability depends on multiple-factors, including the baseline tilting, temperature, electrical field and magnetic field. Here, the baseline tilting issue is addressed by a high order locking scheme, whereas the other issues will be discussed in Section V. Theoretically, the spectral line profile is highly-symmetric [37]. However, the frequency response of the THz spectrometer is not completely flat, and the limited impedance matching at the chip-molecular cell interface introduces a standing wave inside the molecular cell. These cause a tilting in the baseline of the transmission spectrum, as shown in Fig. 3a. In addition, simulated by spectracle [43], the peak absorption intensity of the 231.061 GHz spectral line inside the WR-4.3 waveguide gas cell changes from 49.7% at -40°C to 17.2% at 105°C, while the line width $f_{FWHM}$ increases from 1.17 MHz to 1.33 MHz, as shown in Fig. 4a. Thus, the superposition of the symmetric OCS transition and the tilted baseline results in a temperature-dependent asymmetric line profile (Fig. 3a). As a result, the 1st-order dispersion curve contains an offset-voltage $V_{offset}$ generated from the 1st-order derivative applied on the tilted baseline, and consequently possesses a temperature dependent zero-crossing point as shown in Fig. 3b. Besides the line profile, the slope of the baseline tilting also changes under the PVT variation, partly due to the thermal contraction/expansion of the molecular cell; that further complicates the variation of the zero-crossing point. Therefore, a CSMC locking to the 1st-order dispersion curve suffers from the medium/long-term instability [34].

In comparison, locking to a high-odd-order dispersion curve generates a near-zero offset voltage $V_{offset}$ due to the high-order derivative. As shown in Fig. 3c, the zero-crossing point of the high-odd-order dispersion curve stays invariant under the temperature variation. A numerical simulation of the clock frequency over the slope of the baseline tilting and the temperature variation is conducted in Fig. 4b. Under a fixed baseline tilting of $10^{-4}$ dB/MHz, at 25°C, the 1st and 3rd order locking lead to frequency drifts of $6.5\times10^{-9}$ and $3.4\times10^{-10}$, respectively. A $19\times$ improvement is achieved for the 3rd-order locking. Meanwhile, the baseline-tilting-induced temperature dependencies are $4.9\times10^{-11}$/°C and $0.4\times10^{-12}$/°C for the 1st-order and 3rd-order locking, respectively. The 3rd-order locking reduces the temperature dependency by $126\times$. In addition, due to the simplified baseline model here, the 5th-order locking behaves similarly as the 3rd-order case does. This is also confirmed by the measurement in Table I of Section V-C. Therefore, Fig. 4 does not show the 5th-order results.

We note that the high-order locking was also previously applied in our instrument-based lab-scale OCS clock prototype [27]. In 1970s, Wineland et al., [44], [45] implemented a lab-scale ammonia clock, which referenced to the inversion spectrum of the molecules at 23.8 GHz [46], [47]. Similar high-order locking was adopted. Next, we present our technical details that enable high-order molecular locking in a THz monolithic integrated circuit.

### III. SYSTEM ARCHITECTURE

The system architecture of the CSMC chip is shown in Fig. 5. The key design challenges, as well as the corresponding solutions, are summarized as follows:
(1) Low-power, broadband, and high-quality THz signal generation

The power saturation threshold inside the gas cell of the probing signal is $\sim 50\mu W$ [27]. The power efficiency is critical, since the THz source consumes the majority of the total DC power of CSMC. In addition, the rotational spectrum of OCS exhibits a frequency interval of 12.16 GHz [43]. There are two adjacent lines located at 218.903 GHz and 243.218 GHz, respectively. Due to the PVT issue, the central frequency of CMOS spectroscopic system can differ by $\pm 10\%$. Thus, a wide PLL tuning range (e.g. $\geq 24$ GHz) is preferred. It does not only ensure the spectral line coverage, but also reduces the sensitivity of clock performance over PVT. Furthermore, the phase noise of the probing signal dominates the spectroscopic SNR through a PM-to-AM noise conversion [48]. In this work, driven by a 60 MHz VCXO, a 231 GHz two-stage phase-locked loop (PLL) generates the desired probing signal as shown in Fig. 6.

(2) High-precision THz wavelength modulation

With a MHz-level $\Delta \nu$ and a center frequency $f_0=231.061$ GHz, $f_p$ only fluctuates $\pm 10^{-5}$ for the wavelength modulation. A tunable $\Delta \nu$ is desired to achieve optimal SNR. The frequency distortion of the sinusoidal wavelength modulation also needs to be minimized to avoid the harmonic artifact components in the baseband $I(t)$. In this design, instead of the frequency shift keying (FSK) used in [34]$^1$, a sinusoidal wavelength modulation is realized by applying a digitally-synthesized analog modulation signal onto the voltage-controlled oscillator (VCO) of the 2$^{nd}$-stage PLL (Fig. 7) using a wavelength modulator (WM) (Fig. 8).

(3) Integrated low-loss chip-to-molecular cell interface

The molecular cell hermetically sealed the OCS gas sample inside a 14-cm-long meandering WR-4.3 waveguide. In the 1$^{st}$ CSMC prototype, a pair of lossy ($\approx 10$ dB) off-chip waveguide E-plane quartz probes [49] were used and were the SNR bottleneck [34]. It also results in high assembly variation and manufacturing cost. To solve this issue, a pair of on-chip slot-array couplers (Fig. 12) are innovated with reduced signal loss, enhanced Tx-Rx isolation, and a compact packaging structure. It is a key enabler for a monolithic, low-cost CSMC.

(4) High linearity THz detection

The THz detector and the variable-gain amplifier (VGA) in Fig. 9 convert the FM-modulated intensity fluctuation of THz probing signal to the baseband $I(t)$. The THz receiver chain should have not only high responsivity and low noise equivalent power (NEP), but also high linearity to handle the even-order harmonic components in $I(t)$, which reach peak amplitude at locking (Fig. 2a). Correspondingly, the chip is designed to address the distortion due to saturation (Fig. 9).

(5) Phase-sensitive lock-in detection with low noise and offset

A harmonic rejection lock-in detector (HRLKD) (Fig. 11) demodulates the desired $N^{th}$-order harmonic to DC ($V_{LK,N}$ in Fig. 5). Low output flicker noise of HRLKD is desired to reduce the required gain of preceding VGA and thus improving the Rx linearity. Meanwhile, since the inter-modulation of the lock-in detector would introduce unwanted harmonics and noise, an effective harmonic rejection is preferred. Lastly, the output DC offset of lock-in detector is translated into the clock drift, hence should be minimized.

Finally, after the DC amplification and filtering by off-chip op-amps (GDC in Fig. 5), the error signal $V_{LK,N}$ is fed back to the differential frequency control nodes of VCXO. This way, the chip achieves locking to the zero-crossing point of the $N^{th}$-order dispersion curve. The molecule-regulated 60-MHz VCXO is used as the CSMC output.

IV. DESCRIPTION OF CRITICAL CIRCUIT BLOCKS

In this section, we present the design details of several critical building blocks in Fig. 6.

A. Cascaded Two-Stage 231.061-GHz PLL

The schematic of the 231 GHz cascaded two-stage PLL is shown in Fig. 6. A 60-MHz on-chip VCXO with off-chip quartz crystal [50] is implemented as the PLL reference. It has a frequency tunability of 3 kHz/V and a differential control node for the input common mode noise rejection. The 1$^{st}$-stage 3.21 GHz fractional-N PLL (PLL1) provides a tuning resolution of 24 bit. When the CSMC is locked, it allows for a digitally-set output frequency (around 60 MHz) with a relative frequency step of $6\times 10^{-8}$. Next, referenced to PLL1 (3.21 GHz $\div 16=200.6$ MHz), the 2$^{nd}$-stage integer-N PLL (PLL2) is in charge of high-efficiency, broadband and high-quality THz signal generation. To this end, a cross-coupled 57.77-GHz VCO and a slot-balun [32] based frequency quadrupler ($\times 4$) are adopted in PLL2, as shown in Fig. 7a. The simulation (Fig. 7b) shows a 3-dB power RF bandwidth of 23.4 GHz (26% wider than [34]) and a peak RF power of $-4.4$ dBm ($\sim 2$ x higher than [34]) with a DC power consumption of 46 mW (similar to [34]). In addition, an inductor-less current-mode logic (CML) divider ($\div 8$) is employed to ensure the wideband PLL locking [51].

Compared with the single-stage fractional-N PLL with built-in FSK modulation in [34], the two-stage PLL architecture brings with the following advantages. First, a steady-state,
low frequency fractional-N PLL ensures good frequency resolution, low $\Delta \Sigma$ noise and low spur level. The $\Delta \Sigma$ noise and spur are further reduced by the low-pass filtering of the 2$^{nd}$-stage PLL loop. Second, an analog modulation signal $V_m$ is directly applied to the VCO2 of PLL2 (Fig. 7a), in order to generate a sinusoidal wavelength modulation for the THz detector. In Fig. 6, the cascaded PLL enables a high-order locking. Note that a higher wavelength modulation frequency $f_m$ is desired to reduce the impact of flicker noise in the THz detector. In Fig. 6, the cascaded PLL enables a high $f_m$ of 100 kHz, because the PLL settling time is no longer a limiting factor as that in [34]. Now, $f_m$ is only limited by the molecule linewidth $f_{FWHM}$ [39]. The loop bandwidth of PLL2 is set as 10 kHz for a trade-off between the PLL initial locking (larger bandwidth preferred) and the frequency pulling of the wavelength modulation (smaller bandwidth preferred).

B. High-Precision Wavelength Modulator

The VCO2 in PLL2 (Fig.7a) has two frequency tuning nodes. The VAR1 has a frequency sensitivity of 22.7 GHz/V, which serves for the broadband PLL locking with a 12% locking range. The VAR2 is used for the wavelength modulation ($\pm 10^{-5}$ relative frequency change). For VAR2, a large frequency sensitivity would result in a small signal amplitude of $V_m$. In that case, to maintain a sufficiently high SNR of $V_m$, the modulator needs a higher DC power. It also suffers from a worse spur rejection with a smaller $V_m$. Therefore, besides choosing a minimum-size varactor for VAR2, a resistive source degeneration (Fig. 7a) is used to further reduce the tuning coefficient to 31.3 MHz/V (Fig. 7c). The differential analog modulation signal $V_m$ is digitally-synthesized by a wavelength modulator (WM), as shown in Fig. 8. The WM is clocked by the 60-MHz VCXO. An 8-bit code of the 100-kHz sinusoidal waveform is generated by the digital sine code generator. A phase tunability with 360° range and 0.6° step-size has been included for the phase synchronization of the lock-in detector (HRLKD) is also provided by the WM. Next, the 8-bit code drives a differential digital-to-analog converter (DAC) to generate a rail-to-rail differential sinusoidal signal at $f_m=100$ kHz. After the low-pass filtering, the amplitude of $V_m$ is controlled by the attenuator with a 3-bit control code $D$ for the desired $\Delta f$.

The simulated waveform of the modulation signal $V_m$ are shown in Fig. 8b. The amplitude of $V_m$ is adjustable in a log-scale, as shown in Fig. 8c. The simulated worst case spur rejection (with the minimum $V_m$ amplitude of 25.8 mV while $D=7$) is better than 55 dB, as shown in Fig. 8d. It is noteworthy that both the $V_m$ spurs (which increase with $|V_m|$) and any nonlinearity in the frequency-tuning coefficient of VAR2 (which decreases with $|V_m|$), see Fig. 7c) result in harmonic artifacts in the wavelength modulation, which will be translated into clock frequency drift. In our design, an optimal amplitude of $V_m$ is chosen to minimize such a drift. One future solution is to use a digitally pre-distorted modulation waveform to eliminate the harmonic artifacts. Lastly, the worst case noise floor is 0.32 $\mu$V/$\sqrt{Hz}$ at 1-Hz offset frequency, as shown in Fig. 8e. The associated worst case SNR of the WM is 95 dB, which is sufficiently high to avoid limiting the system overall SNR.

C. THz Detector and Baseband VGA

The schematics of THz square-law detector and variable gain amplifier (VGA) are shown in Fig. 9. A pseudo-differential NMOS transistor pair biased under sub-threshold
Fig. 9: The schematics of THz detector and variable gain amplifier (VGA).

region is used for THz square-law detection. Compared with a single-ended design, it provides better common-mode noise rejection. With a drain current of 49 µA, the simulated responsivity and the noise equivalent power (NEP) of the THz detector, with a 231-GHz input and 100-kHz baseband frequency, are 11.0 kV/W and 11.7 pW/Hz0.5, respectively. The 231.06 GHz probing signal injected into the THz detector has a RF power of ~22 dBm, which induces an output baseband swing of ~23 mV. Thus, the THz detector still works in the small-signal status. The VGA provides 13~65 dB tunable gain to adapt to the baseband output of the THz detector. The VGA consists of two cascaded single-stage op-amps. A high-resistive, transistor-based feedback structure and a 10-pF on-chip capacitor are used to avoid off-chip AC coupling components, and to enhance the isolation of the THz detector and VGA from external interference. In addition, a high loop gain of at least 10^4 is desired for CSMC to suppress the frequency error of VCXO [27]. The VGA is a key contributor to the overall loop gain. However, as shown in Fig. 2a, when locking to the spectral line center (f_p = f_0), in the THz detector output, the near-zero odd-order harmonics at f_m, 3f_m, 5f_m, ⋯ are accompanied with strong even-order harmonics at 2f_m, 4f_m, 6f_m, ⋯. If the gain of VGA is too high, the even-order harmonics drive the VGA to saturation. This is a critical issue that limits the maximum gain of VGA. As a result, the loop gain of CSMC is distributed between the baseband VGA and a DC-gain stage (GDC in Fig. 5). Inside the VGA, a 5-bit resistor bank R0 is used for gain control, and a common-mode feedback (CMFB) circuit is implemented to set the operation point of the output node for large output swing. Another potential solution to address the gain limit of VGA is to use a N-path notch filter [52], which eliminates the even-order harmonics. However, more attentions need to be paid for extra filtering of up-converted harmonics, if this scheme is to be used.

D. Harmonic-Rejection Lock-In Detector (HRLKD)

Conventional lock-in detectors without harmonic rejection [53], [54] suffer from the interference and noise folding at the unwanted harmonics of the reference clock f_ref. That degrades the clock stability. Fig. 10 shows the schematic and phasor diagram of a classic 3rd- and 5th-order harmonic rejection scheme [55], which utilizes switches driven by a
quadrature-phase clock and ratioed transconductance $g_{m}$ to eliminate the 3rd- and 5th-order harmonics of $f_{ref}$. The $g_{m}$ is provided by the MOS transistors biased at saturation region. However, these biased transistors exhibit excessive flicker noise, which cannot be well suppressed due to the limited VGA gain in our CSMC architecture. To solve this issue, a harmonic-rejection lock-in detector (HRLKD) is innovated, as shown in Fig. 10b. It replaces the $g_{m}$ cells with a set of ratioed resistors ($R:R/\sqrt{2}:R$). Similar to the conventional scheme in Fig. 10b, at the $V_{out}$ node, the currents in the three paths recombine constructively when $f_{in}=f_{ref}$, and cancel at $f_{in}=3f_{ref}$ and $f_{in}=5f_{ref}$. The output capacitor $C$ performs additional low-pass filtering. Since resistors and MOS switches exhibit near-zero flicker noise, the proposed HRLKD is better suited for our CSMC. Fig. 11a presents the detailed schematic of the HRLKD. The input of HRLKD is buffered with a source follower for its low output impedance. Meanwhile, differential signaling is used to suppress unwanted even-order-harmonic response, too. The quadrature clock ($f_{ref}=4N \cdot f_{m}$) of HRLKD is obtained from the reference clock generated in the wavelength modulator described previously (Fig. 8a). By specifying the harmonic index $N$, the CSMC can lock to the desired $N$th-order dispersion curve. The simulated harmonic rejection ratio in Fig. 11b is >80 dB for the 2nd- to 6th-order harmonics. The simulated output noise floor is shown in Fig. 11c. Note that the flicker noise of the source follower is upconverted, and is not translated into the output of HRLKD. The current noise floor near DC is dominated by the noise of output resistance $R_{out}$ of HRLKD. Since the ratioed resistors inside the HRLKD adopt $R$ of 100 kΩ, the output resistance $R_{out}$ is 37 kΩ. Next, we note that the output DC offset voltage of the HRLKD also induces clock drift, with a relative clock frequency dependency of $5.0 \times 10^{-11}/\mu V$ in our simulation. Thanks to the 50% duty cycle of the HRLKD clock, the measured output DC offset voltage is lower than 10 μV, and its low sensitivity to temperature causes negligible clock instability. Lastly, we note that the output resistance of HRLKD and the input capacitance of GDC (Fig. 11a) determines the dominant pole of the CSMC feedback control loop. A low dominant pole is achieved by using the Miller capacitor $C_2$ in GDC.

E. Chip-Integrated Slot-Array-Based THz Waveguide Coupler

Low-loss chip-to-molecular cell interface is critical to maintain optimal systematic SNR and to avoid the need for high THz power generation in the CSMC. Prior waveguide E-plane quartz probes [49] and dielectric-resonator-based couplers [56] rely on off-chip components for THz-wave coupling. They present high insertion loss, high assembly cost, and also large sample-to-sample variation. On-chip integrated dipole coupler was demonstrated [57], but it requires not only wafer thinning to tens of μm, but also through-chip vias to suppress the substrate mode, which is not available in many CMOS processes. In this work, a pair of slot array...
couplers are innovated as the chip-to-molecular cell interface. Its 3D structure is shown in Fig. 12a, where four double-slot radiators fed by a slot balun [48] radiate downward into the un-thinned silicon substrate (\(T=304.8 \, \mu m\)). The WR-4.3 metal waveguide opening (\(1.092 \times 0.546 \, \text{mm}^2\)) is attached directly to the backside of the CMOS chip. With optimal slot array dimension, electromagnetic mode matching between the chip-launched fields at the silicon-air interface and the TE_{10} mode in the metal waveguide is achieved and enables efficient coupling.

Fig. 12b shows the simulated electrical-field distribution of the slot array coupler pair. Port 1 and Port 4 are WR-4.3 waveguide with TE_{10} mode. Port 2 and Port 3 are on-chip shielded microstrip line with quasi-TEM mode. The launched waves are concentrated in the substrate, rather than the frontside of the chip, due to the high permittivity of silicon. As a result, the slot array coupler is insensitive to the bond wires and external components on the PCB.

Shown in Fig. 13b, an excellent Tx-to-Rx isolation of 60 dB is obtained in the simulation. In the worst case (90° or 270° phase difference in Fig. 13c), the 60-dB isolation leads to a frequency drift of \(1.8 \times 10^{-9}\) for the 1\(^{st}\)-order locking, and \(0.9 \times 10^{-9}\) for the 3\(^{rd}\)-order locking (Fig. 13d). In the future, even higher isolation in CSMC may be achieved by an active cancellation technique [59]. Since the presented slot-array coupler requires no off-chip component nor wafer thinning, the clock packaging is significantly simplified (more details given in Section V-A).

V. EXPERIMENTAL RESULTS

A. Chip Packaging with Molecular Gas Cell

The chip is fabricated using TSMC 65-nm bulk CMOS technology. The die photo is shown in Fig. 14. The chip has a dimension of \(4 \times 1.25 \, \text{mm}^2\) and an un-thinned (305 \, \mu m), low-resistivity (10 \, \Omega \cdot \text{cm}^{-1}) silicon substrate. The packaged CSMC module is shown in Fig. 15a. It contains an aluminum molecular cell fabricated via computerized numerical control (CNC) milling. The meandering WR-4.3 waveguide has an optimum length of 14 cm for the highest SNR [48]. As shown
Total DC power: 70.4 mW
PLL2 quadrupler: 25.8 mW
PLL2 VCO: 10.5 mW
PLL2 VCO buffer: 9.8 mW
PLL2 CML divider: 13.9 mW
PLL2 TSPC divider, PFD, CP: 2.1 mW
PLL1: 5.0 mW
Rx: 2.4 mW
VCXO: 0.4 mW
WM: 0.5 mW

Fig. 16: The DC power consumption breakdown.

Fig. 17: The measurement results of the spectroscopic Tx and Rx: (a) The measured output RF power versus the simulated RF power including the loss of slot array coupler. (b) The phase noise of 1st-stage PLL at 3.21 GHz and 2nd-stage PLL at 231.061 GHz without modulation. (c) The spectrum of THz probing signal with modulation. Different Δf is applied by specifying the attenuator code D in WM. f0 = 231.061 GHz. (d) The responsivity and noise equivalent power (NEP) of Rx at 231 GHz.

B. Electrical-Performance Characterization of the Chip

The THz output power of the clock module is measured by connecting its WR-4.3 waveguide interface with an Erickson PM-5 power meter. As shown in Fig. 17a, the peak output power, including the loss of slot-array coupler (5.2 dB in simulation), is -9.4 dBm at 231 GHz. The output has a 3-dB bandwidth of 22 GHz (9.5%) and a PLL locking range of 26 GHz (11.3%). The measured output power agrees well with the simulated results, which proves the effectiveness of the slot-array coupler. Next, the phase noise of the 3.21 GHz PLL1 has a volume of $20 \times 16 \times 1.1 \text{ mm}^3$. With micromachined THz waveguide technologies in substrate such as silicon [61], low-cost CSMC with a size of 1 cm$^3$ is feasible. The CSMC chip consumes a total DC power of 70.4 mW, of which a breakdown is given in Fig. 16. Out of that $\sim88\%$ (i.e. 62 mW) is from the PLL2 used for THz power generation. We see a decent room for DC power reduction. For instance, as described in Section IV-E, the generated probing power can be cut by $\sim2\times$ if a high-resistivity silicon substrate is used.

in Fig.15b, the two WR4.3 waveguide apertures of gas cell are sealed by the optically transparent epoxy EPO-TEK 301-2 [60]. To avoid gas leakage and outgassing, the molecular cell is first evacuated to high vacuum through the OCS inlet/outlet with a cut-off frequency much higher than the probing signal to prevent the signal leakage. Next, the standalone gas cell without the CMOS chip is baked under a temperature of 150 °C for 72 hours. Then, OCS molecules are injected with a pressure of 10 Pascal. Lastly, a copper tube connecting the molecular cell with the vacuum system is pinched-off, so as to realize a standalone molecular cell with hermetic sealing (Fig. 15a). The CMOS chip is glued on top of the aluminum base with two waveguide openings of the molecular cell. The special mechanical structure on the aluminum base ensures an alignment tolerance of $\pm 20 \mu m$. Then, the CMOS chip is wire-bonded to a PCB with other periphery circuits (e.g. GDC and the bias circuits). We emphasize that the current packaging is not optimized for minimum form factor. The ultimate limiting factor of the CSMC size is the THz waveguide itself, which

Fig. 15: The packaging of a CSMC module: (a) The gas cell, and CMOS chip bonded on PCB, (b) The hermetically sealed gas cell with optically transparent epoxy.

Pinch off
CMOS chip bonded on PCB
Meandering WR-4.3 waveguide (L=14cm)
output signal, measured by a Keysight N9020A spectrum analyzer, is -96.7 dBc/Hz at 100-kHz offset frequency and -107.5 dBc/Hz at 1-MHz offset frequency (Fig. 17b). The phase noise of the 231.061 GHz PLL2 output, measured through a VDI even-harmonic mixer, is -60.7 dBc/Hz at 100 kHz frequency offset and -81.5 dBc/Hz at 1 MHz frequency offset. This is comparable with the THz sources using coupled oscillator arrays [62], [63], which consume 10× higher DC power. Nevertheless, the associated SNR limit due to a PM-to-AM noise conversion of the spectral line absorption [48] is estimated to be 84 dB. This is currently a major limiting factor of the clock medium-term stability, which will be further discussed in Section V-C. At 231.061 GHz, the measured phase noise is only 2~3 dB worse than the simulation: -62.3 dBc/Hz at 100 kHz frequency offset and -84.9 dBc/Hz at 1 MHz frequency offset. Note that the simulation includes the VCO noise, the thermal noise of gate bias (\(V_{BB}\) in Fig. 7a) and the AM-to-PM noise conversion due to non-linearity of 231 GHz quadrupler, but excludes the power supply noise. Hence, the off-chip power supply noise is one factor that may degrade the PLL performance. As a reference, in this work, Tektronix PWS 4323 with on-broad capacitor array is used to power the chip. Next, after enabling the wavelength modulation, the output spectrum of the probing signal with different \(\Delta f\) are shown in Fig. 17c. The \(\Delta f\) is adjusted through the digital attenuator in Fig. 8.

Finally, the Rx performance is characterized by an external VDI THz source with a tunable \(f_m\) and an Stanford Research System SR865A lock-in amplifier. At \(f_m=100\) kHz, the measured responsivity and noise equivalent power (NEP) achieve 5.5×10^5 V/W and 62.8 pW/√Hz, respectively. A NEP of 19.0 pW/√Hz is derived after de-embedding the loss of the slot array coupler, and such performance is similar to state-of-the-art silicon-based THz detectors [64].

### C. Characterization of the Clock System

The CSMC under an open-loop configuration is used as a spectrometer to measure the 1\(^{st}\)-to-5\(^{th}\)-order dispersion curves. In this configuration, the on-chip Tx and Rx are enabled. A Tx probing signal with \(f_m=100\) kHz and \(\Delta f=2.5\) MHz probes the spectral line in the molecular cell. The frequency deviation \(\Delta f=2.5\) MHz is selected experimentally with the highest SNR×Q product, which is higher than \(\Delta f=1.25\) MHz in Fig. 4 due to the broadening of power saturation effect [37]. By sweeping the PLL frequency, the multi-order dispersion curves are demodulated by the HRLKD, as shown in Fig. 18. Table I summarizes the measured dispersion curve parameters.

<table>
<thead>
<tr>
<th>Order</th>
<th>1(^{st})-order</th>
<th>3(^{rd})-order</th>
<th>5(^{th})-order</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR (dB)</td>
<td>83.5</td>
<td>65.7</td>
<td>58.8</td>
</tr>
<tr>
<td>Amplitude, (V_{amp}) (mV)</td>
<td>165.0</td>
<td>63.8</td>
<td>26.7</td>
</tr>
<tr>
<td>Offset voltage, (V_{offset}) (mV)</td>
<td>1.1</td>
<td>0.0043</td>
<td>0.0012</td>
</tr>
<tr>
<td>(V_{amp}/V_{offset})</td>
<td>150.0</td>
<td>14844</td>
<td>22250</td>
</tr>
</tbody>
</table>

\(^{*}\)The amplitude refers to half of the peak-to-peak voltage in Fig. 18.

![Fig. 18: The measured odd-order dispersion curves under an open loop configuration of CSMC. The measurement setup: \(f_m=100\) kHz and \(\Delta f=2.5\) MHz (\(D=3\)). \(V_{LK,N}\) are the DC output voltages of HRLKD.](image-url)

For the 1\(^{st}\)-to-5\(^{th}\)-order dispersion curves present much lower offset voltage \(V_{offset}\). Even after normalizing \(V_{offset}\) with the different \(V_{amp}\), the 3\(^{rd}\)- and 5\(^{th}\)-order curves are still two orders of magnitude better than the 1\(^{st}\)-order curve. It verifies the effectiveness of high-order probing in dealing with the transmission-baseline tilting. Considering a trade-off between the SNR and the offset voltage \(V_{offset}\), the 3\(^{rd}\)-order dispersion curve is selected for the closed-loop CSMC.

The setup and the measured Allan deviation of the closed-
loop 3rd-order CSMC are shown in Fig. 19. The Allan deviation is measured by a Keysight 53230A frequency counter referenced to a 10-MHz Stanford Research System Rubidium atomic clock (PRS10). With a unity gain loop bandwidth of 5.5 mHz, the 3rd-order CSMC exhibits an Allan deviation of $3.2 \times 10^{-10}$ for an averaging time of $\tau=1$ s and $4.3 \times 10^{-11}$ for an averaging time of $\tau=10^3$ s. Compared with the free running VCXO, the medium/long-term stability at $\tau=10^3$ s is improved by almost three orders of magnitude. Fig. 20a shows the measurement setup for the clock temperature dependency and the magnetic field sensitivity. The temperature is controlled by a heater beneath the CSMC. Without any temperature compensation, the CSMC frequency drifts by $\pm 5 \times 10^{-8}$ over a temperature range of 27°C to 65°C (Fig. 20b). With an on-chip temperature sensor (Fig. 5) and a simple 2nd-order polynomial compensation, the clock drift is reduced to $\pm 3 \times 10^{-9}$, as shown in Fig. 20c. It should be noted that the current temperature measurement range is limited by the test setup and the ability to dynamically adjust the bias current (especially for the CML divider in Fig.6) to maintain the clock locking. Assuming these technical issues can be solved in the future, it is expected that the compensated frequency over the full temperature range (-10°C to 70°C) should be comparable to the presented value. Furthermore, note that the frequency stability shown in Fig. 19 has no temperature compensation. A long-term stability measurement with up to $\tau=10^5$s has also been conducted, with an Allan deviation result of $8.8 \times 10^{-11}$ using the 2nd-order polynomial compensation similar to that in Fig. 20b. With our ongoing improvement of the gas cell quality and development of clock architectures with built-in real-time compensation, performance at even longer term (e.g. $\tau = 10^5$s) will be investigated in the future.

Finally, it is noteworthy that the CSMC is by principle insensitive to external magnetic field variation [35], because the rotational spectral lines only respond to the 2nd-order Zeeman shift and its gyromagnetic factor (i.e. g-factor) is much lower than that in CSACs. To verify this, a 75-Gauss magnetic field is applied every other 3 minutes via a custom-made Helmholtz coil (Fig. 20a). As shown in Fig. 20d, a corresponding frequency fluctuation of $\sim 4 \times 10^{-10}$ is observed from the CSMC. That is equivalent to a very low magnetic-field sensitivity of $\pm 2.9 \times 10^{-12}$ Gauss$^{-1}$.

VI. CONCLUSION

The transmission baseline tilting is a key issue that results in the medium/long-term frequency drift of CSMCs. In this work, a high-odd-order CSMC on 65 nm CMOS technology is innovated. It effectively reduces the impact of the transmission baseline tilting by locking to a high-odd-order dispersion curve of wavelength-modulation spectroscopy. Table II compares the high-order CSMC with other high-stability, miniaturized clocks. Firstly, the all-electronic CSMC marks a dramatic cost reduction compared to CSACs due its CMOS chip core and simplified package. Next, with an improved spectroscopic system and high-order locking scheme, the clock stability at $\tau=1$ s and $\tau=10^3$ s is improved by $8 \times$ and $9 \times$, respectively, comparing to the first CSMC prototype [34]. In addition, an excellent temperature stability of $\pm 3 \times 10^{-9}$ is achieved without using oven-controlled temperature stabilization. Fur-
thermore, without any magnetic shield, the magnetic field sensitivity of the high-order CSMC is $30 \times$ less than the state-of-the-art CSACs with dedicated shields. Also note that CSMCs have faster start-up time, because no Alkali evaporation and temperature stabilization as those in CSACs are needed. Lastly, a competitive 70.4 mW power consumption of the presented CSMC makes it suitable for power-constraint applications. It should be noted that, as an emerging technology, the CSMCs still have vast room for performance and efficiency improvement. That is particularly justified with the recent advances in CMOS processes, which now offer transistors with $f_{max}$ around 400 GHz [65], [66]. Therefore, a CSMC with atomic-clock-grade stability, cm$^3$ volume and <$50$-mW DC power becomes feasible in the near future.

ACKNOWLEDGMENT

The authors appreciate the help from Dr. Stephen Coy, Prof. Robert Field, Prof. Keith Nelson from the Department of Chemistry, MIT, Prof. John Muenter from the Department of Chemistry, University of Rochester, and Dr. Bradford Perkins from MIT Lincoln Laboratories. They also acknowledge the technical discussions with Dr. Dennis Bus and Dr. Juan Herbsommer at Texas Instruments Kilby Laboratory, Prof. Hae-Seung Lee at MIT, Dr. Lin Yi at NASA Jet Propulsion Laboratory, and Dr. Cort Johnson at Draper Laboratory.

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