

A Terahertz Molecular Clock on CMOS Using High-Harmonic-Order Interrogation of Rotational Transition for Medium-/Long-Term Stability Enhancement

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Abstract—Chip-scale molecular clocks (CSMCs) perform frequency stabilization by referencing to the rotational spectra of polar gaseous molecules. With, potentially, the “atomic” clock grade stability, cm³-level volume, and <100-mW dc power, CSMCs are highly attractive for the synchronization of the high-speed radio access network (RAN), precise positioning, and distributed array sensing. However, the medium-/long-term stability of CSMCs is hindered by the transmission baseline tilting due to the uneven frequency response of the spectroscopic system and the molecular cell. To enhance the medium-/long-term stability, this article presents a CSMC architecture locking to the high-odd-order dispersion curve of the 231.061-GHz rotational spectral line of carbonyl sulfide (OCS) molecules, which is selected as the clock reference. A monolithic THz transceiver generates a high-precision, wavelength-modulated probing signal. Then, the wave-molecule interaction inside the molecular cell translates the frequency error between the probing signal and the spectral line center to the periodic intensity fluctuation. Finally, the CSMC locks to the third-order dispersion curve after a phase-sensitive lock-in detection. In addition, a pair of slot array couplers is employed as an effective chip-to-molecular cell interface. It leads to not only a higher SNR but also a significantly simplified CSMC package. Implemented on a 65-nm CMOS process, the high-order CSMC presents a measured Allan deviation of 4.3×10^{-11} under an averaging time of $\tau = 10^3$ s while consuming 70.4-mW dc power.

Index Terms—Allan deviation, carbonyl sulfide (OCS), chip-scale molecular clock (CSMC), CMOS, frequency stability, high-order dispersion curve, rotational spectroscopy.

Manuscript received March 30, 2020; revised July 18, 2020 and August 27, 2020; accepted August 31, 2020. Date of publication September 16, 2020; date of current version January 28, 2021. This article was approved by Associate Editor Pietro Andreani. This work was supported in part by the National Science Foundation under Grant CAREER ECCS-1653100 and Grant ECCS-1809917, in part by the MIT Lincoln Laboratory under Grant ACC-672, in part by the Texas Instruments Fellowship, in part by the Kwangjeong Scholarship, and in part by the NASA Jet Propulsion Laboratory. This article was presented at the International Solid-State Circuit Conference (ISSCC), San Francisco, CA, USA, February 2020. (Corresponding author: Ruonan Han.)

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Digital Object Identifier 10.1109/JSSC.2020.3021335

I. INTRODUCTION

HIGHLY stable, miniaturized, power-efficient, and low-cost clocks are increasingly important for the emerging electronics. For instance, augmented/virtual reality (AR/VR) devices, real-time multi-person online gaming, and autonomous driving all require radio access networks (RANs) with high capacity (~ 1 -Gbit/s throughput per node), high density (one million nodes per km²), and low latency (1 \sim 10 ms) [1], [2]. It leads to the stringent requirements for clock synchronization. For example, the international telecommunication union (ITU) specifies a maximum relative timing error of 65 ns for the massive multi-input-multi-output (MIMO) systems of 5G new radio (NR) [3]. Furthermore, the positioning service through 5G base stations demands a 10-ns relative timing error for a 3-m accuracy [1]. However, only a μ s-level timing accuracy has been provided for the current 4G-LTE base stations relying on the precision timing protocol (PTP) with the global positioning system (GPS) [4]. On top of that, it is worth mentioning that the GPS accuracy degradation and signal blockage commonly occur in urban areas and indoor environments, where 5G NR base stations are to be deployed [5]. In addition, the cost of synchronization networks is also critical. On the one hand, compact 5G base stations are heavily densified due to the high data throughput and the limited signal coverage [6]; on the other hand, a significant cost reduction per unit bandwidth at the user end is expected. The usage of traditional atomic clocks, which are bulky and expensive, as the backbone of synchronization networks becomes problematic [7], calling for new high-stability clocks with low cost and small size. Another potential application of these clocks is the ocean bottom seismographs for oil exploration [8]–[10]. The massive acoustic sensor networks reconstruct the geometric structure beneath the ocean floor according to the precise arrival time of the reflected sonic pulses. The acoustic sensors experience tens of Celsius of temperature variation while sinking to the ocean floor. Meanwhile, powered by batteries, they stay under a GPS-denial environment for up to a year. To keep the required timing accuracy of 1 \sim 10 ms over this period, the sensor clock should provide stability at 10^{-11} level while keeping its power low.

Existing technologies do not completely fulfill the current needs. The widely adopted oven-compensated crystal oscillators (OCXOs) [11], [12] and MEMS oscillators (OCMOs) [13]–[15] isolate the resonators from the surrounding environment using a heated oven. The clock frequency is further regulated by the temperature compensation [16], [17]. The OCXO/OCMO provide decent temperature stability of $10^{-7} \sim 10^{-8}$ over the full temperature range ($-20^\circ\text{C} \sim +70^\circ\text{C}$) [11], [12]. However, their dc power is at watt level in steady-state and is even higher during startup. Alternatively, chip-scale atomic clocks have been developed [18]–[20]. They are referenced to the electronic transitions of Alkali atoms [e.g., rubidium (^{85}Rb) or Cesium (^{133}Cs)]. The utility of coherent population trapping (CPT) [21] and micro-fabricated vapor cell [22] enables significant miniaturization and power reduction. The CSAC in [23] achieves a stability of $\pm 1 \times 10^{-9}$ within $-10^\circ\text{C} \sim +70^\circ\text{C}$ while only consuming 60-mW dc power. However, the CSACs possess several disadvantages.

- 1) A high cost due to sophisticated optical-electrical construction. The required vertical cavity surface emitting laser (VCSEL) with precise 894.6-nm (D1) or 852.3-nm (D2) laser wavelength for ^{133}Cs atom probing has low yield [24]. Advanced MEMS and packaging technologies are applied for the tight integration of VCSEL, laser detector, micro-fabricated vapor cell, and microwave circuitry.
- 2) Susceptibility to external magnetic fields due to the strong magnetic dipole of electron spins. As a result, all CSACs are equipped with a magnetic shield to alleviate the problem [25].
- 3) A slow startup procedure. After a cold start, the clock package should be heated to around 80°C for Alkali metal evaporation and then temperature-stabilized with mK-level accuracy to ensure precise laser wavelength. For instance, the Microsemi SA.45s CSAC needs 3 min for its startup procedure [26].

Recently, the rotational spectra of polar gaseous molecules in the terahertz range emerge as new physical references for clock stabilization [27]. A rotational spectral line could have a high quality factor ($\sim 10^6$) and strong absorption intensity. Meanwhile, THz spectrometers on CMOS have been demonstrated [28]–[32]. Thus, low-cost clocks at chip scale and with “atomic” clock grade stability become possible. The first chip-scale molecular clock (CSMC) chipset on 65-nm CMOS locks to the 231.061-GHz rotational spectral line of carbonyl sulfide ($^{16}\text{O}^{12}\text{C}^{32}\text{S}$) molecules in gas phase [33], [34]. It presents an Allan deviation of $\sigma_y = 3.8 \times 10^{-10}$ with an averaging time $\tau = 10^3$ s and a 66-mW dc power. It enables a fast startup and all-electronic configuration potentially leading to dramatic cost reduction compared with CSACs. However, its medium-/long-term stability with the presence of temperature fluctuation is degraded by the tilting of its spectroscopic transmission baseline. Such tilting is caused by the inevitable, uneven frequency response of the THz spectrometer and the molecular cell. In Section II, we show that it leads to a spectral line profile with a temperature-dependent asymmetry, which cannot be corrected by the

first-order dispersion curve probing approach adopted by the CSMC [34], [35].

In this article, a new CSMC locking to a high-odd-order dispersion curve is demonstrated [36]. It also references the 231.061-GHz spectral line of OCS molecules. By performing a third-order derivative on the asymmetric line profile, the new dispersion curve generated by the clock exhibits less temperature dependence, and thus, the medium-/long-term stability of the clock is significantly improved. In this 65-nm CMOS chip, a high-order spectroscopic system is implemented with enhanced sensitivity and signal purity. In the experiments, the CSMC achieves Allan deviations of $\sigma_y = 3.2 \times 10^{-10}$ @ $\tau = 1$ s and $\sigma_y = 4.3 \times 10^{-11}$ @ $\tau = 10^3$ s. Compared with the prior CSMC [34], [35], an $\sim 8\times$ stability improvement is obtained with a similar dc power of 70.4 mW. In addition, a single-chip realization is achieved through employing a pair of slot array couplers as an effective chip-to-molecular cell interface. It results in further packaging simplification and cost reduction. This article is organized as follows. In Section II, the impacts of transmission baseline tilting and the high-order molecular probing scheme are illustrated. In Section III, the architecture of CSMC enabling the probing scheme is presented. Section IV discusses the details of the circuit blocks. Then, Section V presents the clock packaging and the experiment results. Section VI concludes this article with a comparison with the other state-of-the-art time-keeping devices.

II. TRANSMISSION BASELINE TILTING AND HIGH-ODD-ORDER DISPERSION CURVES

A simplified schematic of CSMCs is shown in Fig. 1(a). A wavelength modulated THz probing signal $V_{\text{WM}}(t)$ is generated by a THz transmitter (Tx) referenced to a voltage-controlled crystal oscillator (VCXO). The VCXO determines the short-term clock stability [see Fig. 1(b)]. The instantaneous frequency $f_p(t)$ [see Fig. 2(a)] of $V_{\text{WM}}(t)$ is expressed as

$$f_p(t) = f_p + \Delta f \sin(2\pi f_m t) \quad (1)$$

where f_p is the center frequency, f_m is the modulation frequency, and Δf is the frequency deviation. The gas absorption coefficient $\alpha(f)$ of the selected spectral line has a Lorentzian profile due to the pressure broadening [37], [38], which can be decomposed into a complex form as follows:

$$\begin{aligned} \alpha(f) &= \alpha_p \frac{f_h^2}{f_h^2 + (f - f_0)^2} \\ &= \beta \left[\frac{1}{f_h + (f - f_0)i} + \frac{1}{f_h - (f - f_0)i} \right] \end{aligned} \quad (2)$$

where α_p is the peak absorption coefficient in the spectral line center f_0 , f_h is the half-width at half-maximum of a specific spectral line, and the coefficient $\beta = \alpha_p f_h / 2$. After the wave-molecule interaction, the intensity of the probing signal is periodically modulated, as shown in Fig. 2(a). Then, a THz square-law detector [see Fig. 1] converts the intensity fluctuation into the baseband signal $I(t)$

$$\begin{aligned} I(t) &= I_0 \cdot e^{-\alpha(f_p(t))L} \\ &\approx I_0 \cdot (1 - \alpha(f_p + \Delta f \sin(2\pi f_m t))L) \end{aligned} \quad (3)$$

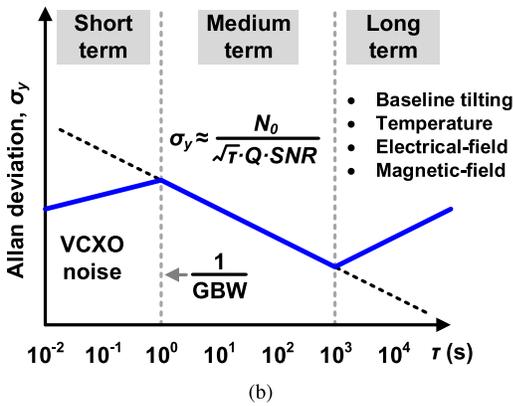
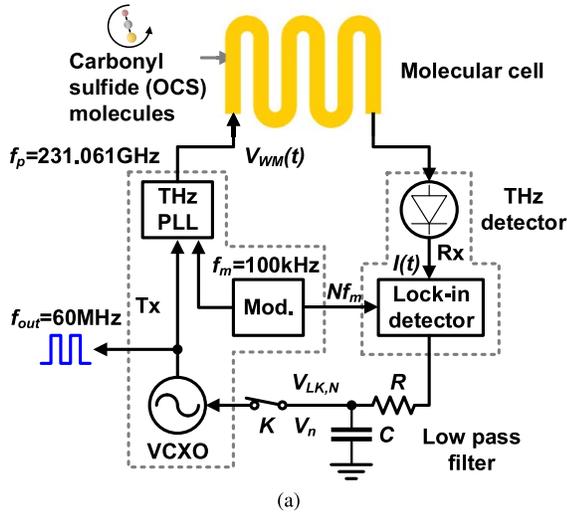


Fig. 1. High-order molecular probing CSMC. (a) Simplified schematic. (b) Clock stability in the short, medium, and long terms.

where I_0 is the baseband signal without the gas absorption, and L refers to the path length of the molecular cell. $\alpha(f)L \ll 1$ is assumed in (3). Note that $I(t)$ has abundant harmonics of f_m . Correspondingly, (3) can be decomposed as

$$I(t) \approx I_0 \left[1 - \sum_{n=0}^{\infty} V_{LK,N}(f_p) \cos(2\pi N f_m t) \right] \quad (4)$$

where $V_{LK,N}(f_p)$ is the N th Fourier component of the baseband signal at f_p . $N \in \{1, 2, \dots, \infty\}$. By assuming $\Delta f \ll f_{FWHM}$, where $f_{FWHM} = 2f_h$ is the full-width at half-maximum of the spectral line, and $V_{LK,N}(f_p)$ can be expressed as [39], [40]

$$V_{LK,N}(f_p) \propto L \frac{2^{1-N}}{N!} \Delta f^n \left. \frac{d^N \alpha(f)}{df^N} \right|_{f=f_p} \quad (5)$$

$V_{LK,N}(f_p)$ is proportional to the N th-order derivative of $\alpha(f)$ in (5). In Fig. 1(a), with the switch K “open,” $V_{LK,N}(f_p)$ is measured by a phase-sensitive lock-in detector. By sweeping f_p , $V_{LK,N}(f_p)$ can be recorded as the N th-order dispersion curve [see Fig. 2(b)]. The N th-order derivative of the gas

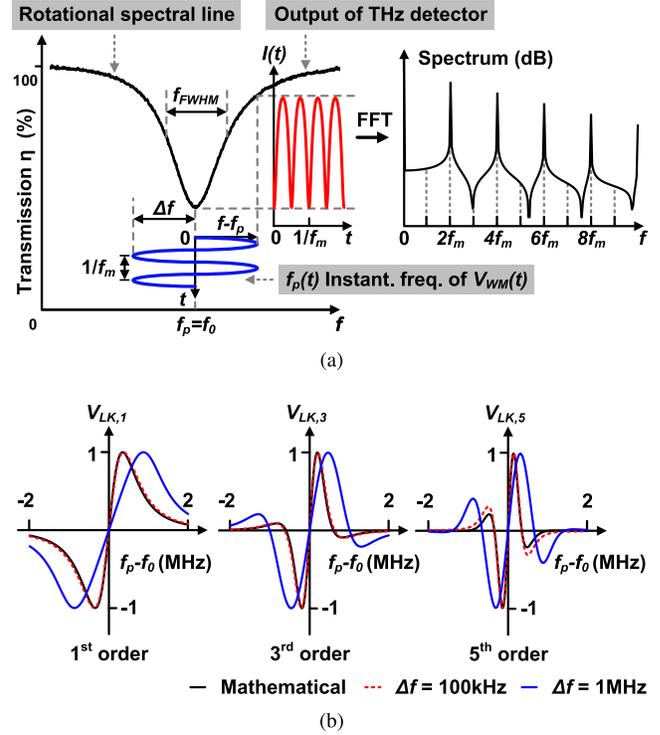


Fig. 2. WMS. (a) Harmonic generation while probing the spectral line with a wavelength-modulated signal. (b) Mathematical derivatives of the Lorentz profile and the simulated odd-order dispersion curves with $\Delta f = 100$ kHz and 1 MHz, respectively. $f_m = 0.1 \times \Delta f$. The amplitude is normalized. The polarization is aligned for a better comparison.

absorption coefficient $\alpha(f)$ in (2) can be expressed as

$$\frac{d^N \alpha(f)}{df^N} = N! \cdot i^N \cdot \beta \cdot \left[\frac{(-1)^N}{(f_h + (f - f_0)i)^{N+1}} + \frac{1}{(f_h - (f - f_0)i)^{N+1}} \right] \quad (6)$$

While the center frequency of probing signal coincides with the spectral line center $f_p = f_0$, (6) can be written as

$$\left. \frac{d^N \alpha(f)}{df^N} \right|_{f=f_p=f_0} = \frac{N! \cdot i^N \cdot \beta}{f_h^{N+1}} ((-1)^N + 1) \quad (7)$$

As a result, while $f_p = f_0$, all the odd-order derivatives equal 0. Accordingly, (5) indicates that the baseband signal $I(t)$ only has even order harmonics of f_m , which is shown in Fig. 2(a). Since $V_{LK,N}(f_p)$ is 0 for all the odd-order harmonics, the odd-order dispersion curves exhibit a zero-crossing point at $f_p = f_0$ [see Fig. 2(b)], which provides the amplitude and polarization of frequency feedback control. Hence, the odd-order dispersion curves can be adopted in CSMCs [27]. With a small frequency deviation [e.g., $\Delta f = 100$ kHz $\ll f_{FWHM} = 1.47$ MHz [34] in Fig. 2(b)], the dispersion curves match well with the mathematical N th-order derivative of the spectral line profile. However, a large Δf is generally used for a higher loop gain and SNR. As shown in Fig. 2(b), the dispersion curves deviate from the math with $\Delta f = 1$ MHz. For more details on wavelength modulation spectroscopy (WMS) with a large Δf , Wahlquist [41] and Arndt [42] gave thorough analyses. Then, by “closing” the

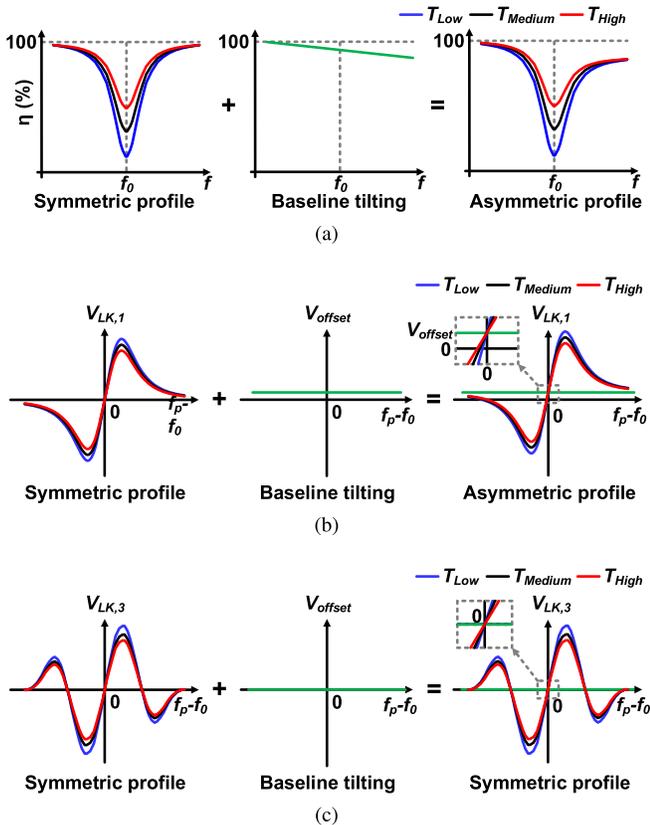


Fig. 3. Baseline tilting induced frequency drift. (a) Asymmetric spectral line profile due to the baseline tilting. (b) First-order dispersion curve shifted by the offset voltage V_{offset} due to the baseline tilting. (c) High-order dispersion curve stands invariant under the baseline tilting. T_{high} , T_{medium} , and T_{low} stand for the high, medium, and low temperatures.

switch K in Fig. 1(a), the CSMC locks to the zero-crossing point $f_p = f_0$ of the selected odd-order dispersion curve. After the locking, the clock stability in the medium term is inversely proportional to the $Q \times \text{SNR}$ product [27] [see Fig. 1(b)], where Q refers to the quality factor of the spectral line. With a fixed Q , a CSMC with higher SNR presents better medium-term stability.

Fig. 1(b) reveals that the clock medium-/long-term stability depends on multiple factors, including the baseline tilting, temperature, electrical field, and magnetic field. Here, the baseline tilting issue is addressed by a high-order locking scheme, whereas the other issues will be discussed in Section V. Theoretically, the spectral line profile is highly symmetric [37]. However, the frequency response of the THz spectrometer is not completely flat, and the limited impedance matching at the chip-molecular cell interface introduces a standing wave inside the molecular cell. These cause a tilting in the baseline of the transmission spectrum, as shown in Fig. 3(a). In addition, simulated by spectralcalc [43], the peak absorption intensity of the 231.061-GHz spectral line inside the WR-4.3 waveguide gas cell changes from 49.7% at -40°C to 17.2% at 105°C , while the linewidth f_{FWHM} increases from 1.17 to 1.33 MHz, as shown in Fig. 4(a). Thus, the superposition of the symmetric OCS transition and the tilted baseline results in a temperature-dependent asymmetric line profile [see Fig. 3(a)]. As a result, the first-order dispersion curve contains an offset-voltage

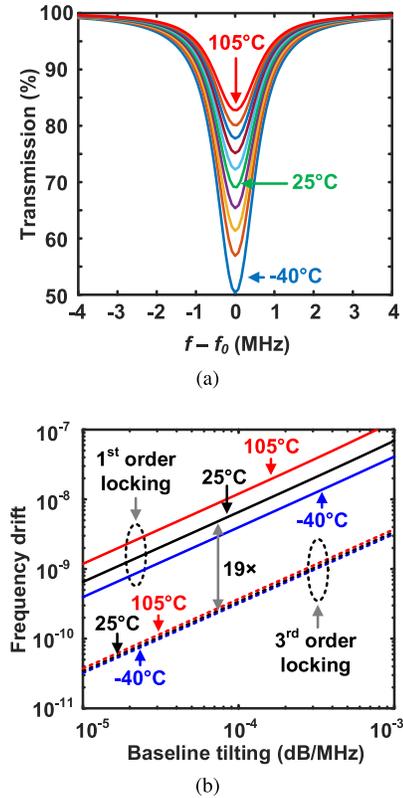


Fig. 4. Temperature dependence of molecular clock. (a) Simulated 231.061-GHz line profile inside the gas cell under -40°C – 105°C . (b) Simulated frequency tilting of the first- and third-order lockings of CSMCs under: 1) a baseline tilting of 10^{-5} – 10^{-3} dB/MHz (or 0.01–1 dB/GHz, which is common in the THz transceivers) and 2) a temperature variation of -40°C – 105°C . In the simulation, $f_m = 100$ kHz, and $\Delta f = 1.25$ MHz.

V_{offset} generated from the first-order derivative applied on the tilted baseline and consequently possesses a temperature-dependent zero-crossing point, as shown in Fig. 3(b). Besides the line profile, the slope of the baseline tilting also changes under the PVT variation, partly due to the thermal contraction/expansion of the molecular cell, which further complicates the variation of the zero-crossing point. Therefore, a CSMC locking to the first-order dispersion curve suffers from the medium-/long-term instability [34].

In comparison, locking to a high-odd-order dispersion curve generates a near-zero offset voltage V_{offset} due to the high-order derivative. As shown in Fig. 3(c), the zero-crossing point of the high-odd-order dispersion curve stays invariant under the temperature variation. A numerical simulation of the clock frequency over the slope of the baseline tilting and the temperature variation is conducted in Fig. 4(b). Under a fixed baseline tilting of 10^{-4} dB/MHz, at 25°C , the first- and third-order lockings lead to frequency drifts of 6.5×10^{-9} and 3.4×10^{-10} , respectively. A 19 \times improvement is achieved for the third-order locking. Meanwhile, the baseline-tilting-induced temperature dependencies are $4.9 \times 10^{-11}/^\circ\text{C}$ and $0.4 \times 10^{-12}/^\circ\text{C}$ for the first- and third-order lockings, respectively. The third-order locking reduces the temperature dependence by 126 \times . In addition, due to the simplified baseline model here, the fifth-order locking behaves similarly as the third-order case does. This is also confirmed by the

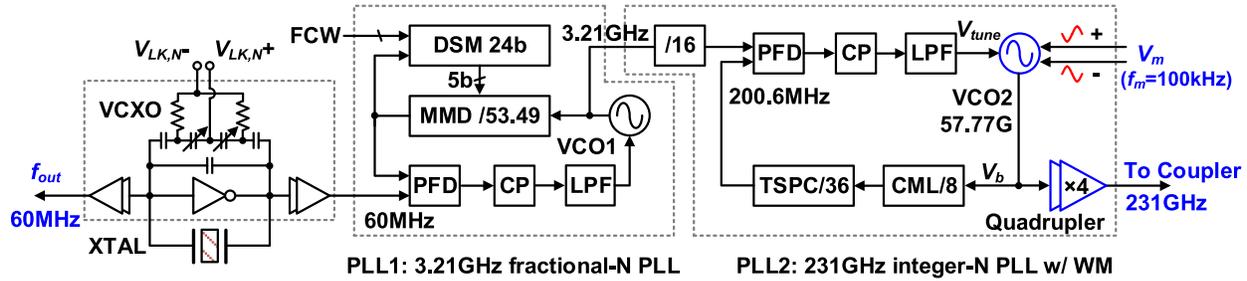


Fig. 6. Schematic of cascaded two-stage 231.061-GHz PLL with a 60-MHz on-chip VCXO.

A. Cascaded Two-Stage 231.061-GHz PLL

The schematic of the 231-GHz cascaded two-stage PLL is shown in Fig. 6. A 60-MHz on-chip VCXO with off-chip quartz crystal [50] is implemented as the PLL reference. It has a frequency tunability of 3 kHz/V and a differential control node for the input common-mode noise rejection. The first-stage 3.21-GHz fractional- N PLL (PLL1) provides a tuning resolution of 24 bit. When the CSMC is locked, it allows for a digitally set output frequency (around 60 MHz) with a relative frequency step of 6×10^{-8} . Next, referenced to PLL1 ($3.21 \text{ GHz} \div 16 = 200.6 \text{ MHz}$), the second-stage integer- N PLL (PLL2) is in charge of high-efficiency, broadband, and high-quality THz signal generation. To this end, a cross-coupled 57.77-GHz VCO and a slot-balun-based frequency quadrupler ($\times 4$) [32] are adopted in PLL2, as shown in Fig. 7(a). The simulation [see Fig. 7(b)] shows a 3-dB power RF bandwidth of 23.4 GHz (26% wider than [34]) and a peak RF power of -4.4 dBm ($\sim 2\times$ higher than [34]) with a dc power consumption of 46 mW (similar to [34]). In addition, an inductor-less current-mode logic (CML) divider ($\div 8$) is employed to ensure the wideband PLL locking [51].

Compared with the single-stage fractional- N PLL with built-in FSK modulation in [34], the two-stage PLL architecture brings the following advantages. First, a steady-state, low-frequency fractional- N PLL ensures good frequency resolution, low Δ - Σ noise, and low spur level. The Δ - Σ noise and spurs are further reduced by the low-pass filtering of the second-stage PLL loop. Second, an analog modulation signal V_m is directly applied to the VCO2 of PLL2 [see Fig. 7(a)] in order to generate a sinusoidal wavelength modulation for the high-order locking. Note that a higher wavelength modulation frequency f_m is desired to reduce the impact of flicker noise in the THz detector. In Fig. 6, the cascaded PLL enables a high f_m of 100 kHz because the PLL settling time is no longer a limiting factor like that in [34]. Now, f_m is only limited by the molecule linewidth f_{FWHM} [39]. The loop bandwidth of PLL2 is set as 10 kHz for a tradeoff between the PLL initial locking (larger bandwidth preferred) and the frequency pulling of the wavelength modulation (smaller bandwidth preferred).

B. High-Precision Wavelength Modulator

The VCO2 in PLL2 [see Fig. 7(a)] has two frequency-tuning nodes. The VAR1 has a frequency sensitivity of 22.7 GHz/V, which serves for the broadband PLL locking with

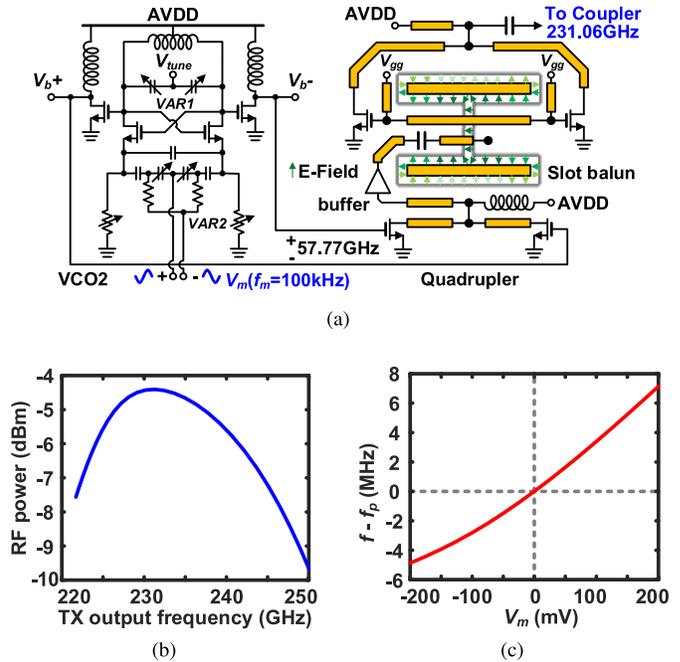


Fig. 7. 57-GHz VCO and 231-GHz quadrupler of PLL2. (a) Schematic. (b) Simulated RF output power and tuning range. (c) Simulated frequency sensitivity of wavelength modulation through VAR2.

a 12% locking range. The VAR2 is used for the wavelength modulation ($\pm 10^{-5}$ relative frequency change). For VAR2, a large frequency sensitivity would result in a small signal amplitude of V_m . In that case, to maintain a sufficiently high SNR of V_m , the modulator needs a higher dc power. It also suffers from a worse spur rejection with a smaller V_m . Therefore, besides choosing a minimum-size varactor for VAR2, a resistive source degeneration [see Fig. 7(a)] is used to further reduce the tuning coefficient to 31.3 MHz/V [see Fig. 7(c)]. The differential analog modulation signal V_m is digitally synthesized by a WM, as shown in Fig. 8. The WM is clocked by the 60-MHz VCXO. An 8-bit code of the 100-kHz sinusoidal waveform is generated by the digital sine code generator. A phase tunability with 360° range and 0.6° step size has been included for the phase synchronization of the lock-in demodulation in Rx. A reference clock $f_{\text{ref}} = 4 \cdot N \cdot f_m$ for the lock-in detector (HRLKD) is also provided by the WM. Next, the 8-bit code drives a differential digital-to-analog converter (DAC) to generate a rail-to-rail differential

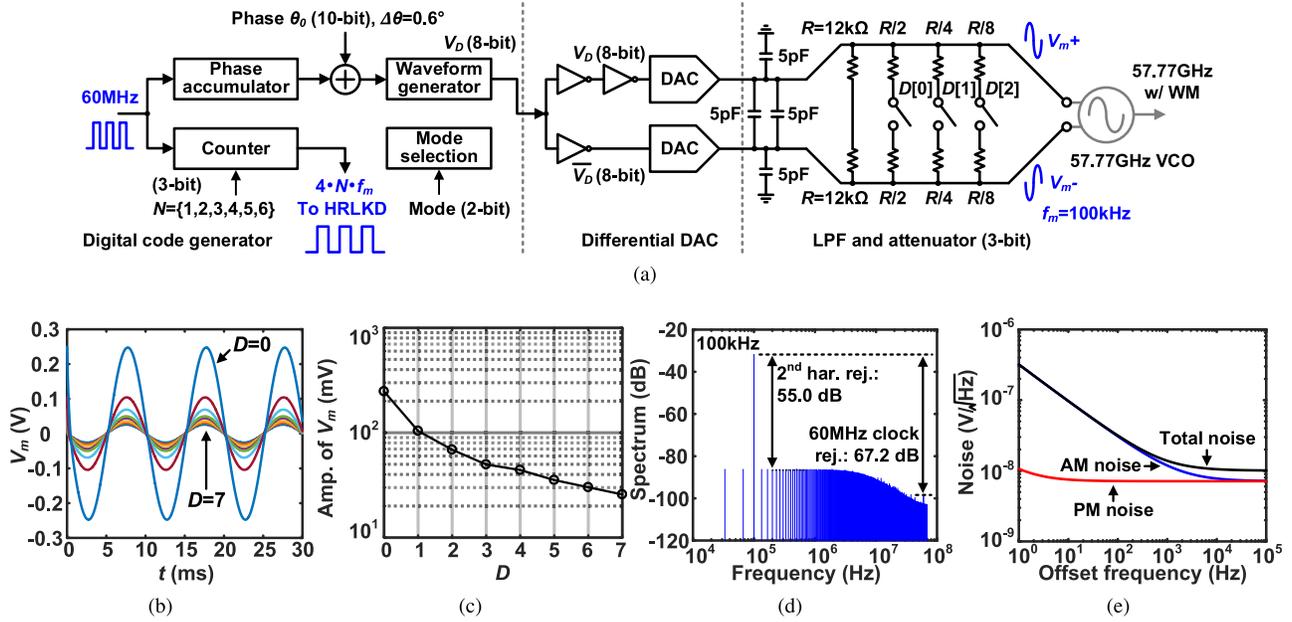


Fig. 8. WM. (a) Schematic. (b) Simulated V_m waveform. (c) Amplitude of V_m versus the control code D . (d) Simulated spectrum of V_m while $D = 7$. (e) Simulated noise voltage of the 100-kHz modulation signal, while $D = 7$.

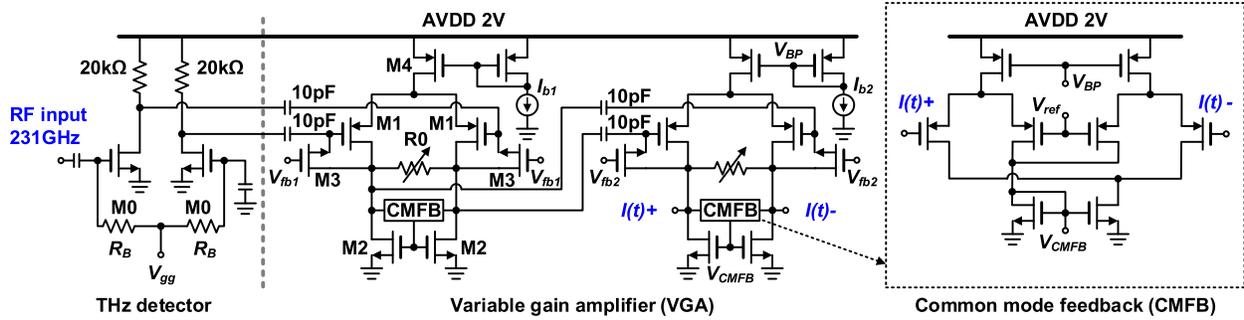


Fig. 9. Schematics of THz detector and VGA.

sinusoidal signal at $f_m = 100$ kHz. After the low-pass filtering, the amplitude of V_m is controlled by the attenuator with a 3-bit control code D for the desired Δf .

The simulated waveform of the modulation signal V_m is shown in Fig. 8(b). The amplitude of V_m is adjustable in a log-scale, as shown in Fig. 8(c). The simulated worst case spur rejection (with the minimum V_m amplitude of 25.8 mV, while $D = 7$) is better than 55 dB, as shown in Fig. 8(d). It is noteworthy that both the V_m spurs (which increase with $|V_m|$) and any nonlinearity in the frequency-tuning coefficient of VAR2 [which decreases with $|V_m|$, see Fig. 7(c)] result in harmonic artifacts in the wavelength modulation, which will be translated into clock frequency drift. In our design, an optimal amplitude of V_m is chosen to minimize such a drift. One future solution is to use a digitally pre-distorted modulation waveform to eliminate the harmonic artifacts. Finally, the worst case noise floor is $0.32 \mu\text{V}/\sqrt{\text{Hz}}$ at 1-Hz offset frequency, as shown in Fig. 8(e). The associated worst case SNR of the WM is 95 dB, which is sufficiently high to avoid limiting the system overall SNR.

C. THz Detector and Baseband VGA

The schematics of the THz square-law detector and VGA are shown in Fig. 9. A pseudo-differential nMOS transistor pair biased under the sub-threshold region is used for THz square-law detection. Compared with a single-ended design, it provides better common-mode noise rejection. With a drain current of $49 \mu\text{A}$, the simulated responsivity and the NEP of the THz detector, with a 231-GHz input and 100-kHz baseband frequency, are 11.0 kV/W and $11.7 \text{ pW/Hz}^{0.5}$, respectively. The 231.06-GHz probing signal injected into the THz detector has an RF power of ~ -22 dBm, which induces an output baseband swing of ~ 23 mV. Thus, the THz detector still works in the small-signal status. The VGA provides 13~65-dB tunable gain to adapt to the baseband output of the THz detector. The VGA consists of two cascaded single-stage op-amps. A high-resistive, transistor-based feedback structure and a 10-pF on-chip capacitor are used to avoid off-chip ac coupling components and enhance the isolation of the THz detector and VGA from external interference. In addition, a high loop gain of at least 10^4 is desired for CSMC to suppress the frequency error of VCXO [27]. The VGA is a

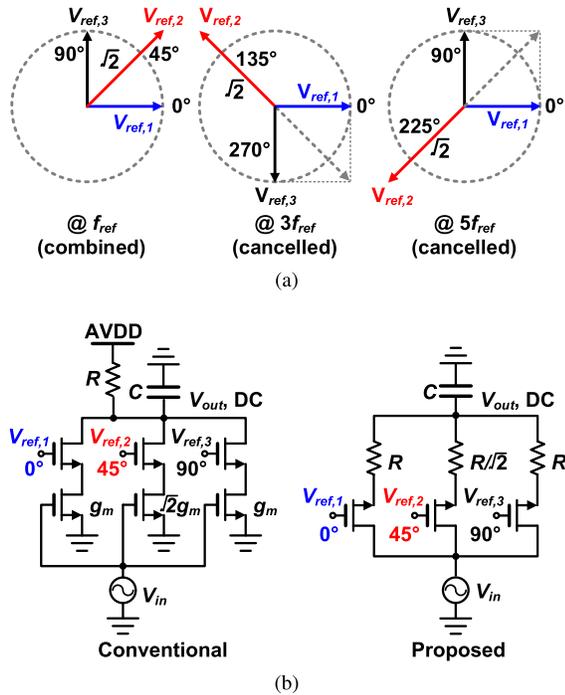


Fig. 10. Harmonic-rejection scheme. (a) Phasor diagram of the classic third- and fifth-order harmonic-rejection schemes. (b) Comparison between the conventional harmonic-rejection mixer and the proposed resistive-based lock-in detector.

key contributor to the overall loop gain. However, as shown in Fig. 2(a), when locking to the spectral line center ($f_p = f_0$), in the THz detector output, the near-zero odd-order harmonics at f_m , $3f_m$, $5f_m$, ... are accompanied with strong even-order harmonics at $2f_m$, $4f_m$, $6f_m$, ... If the gain of VGA is too high, the even-order harmonics drive the VGA to saturation. This is a critical issue that limits the maximum gain of VGA. As a result, the loop gain of CSMC is distributed between the baseband VGA and a dc-gain stage (GDC in Fig. 5). Inside the VGA, a 5-bit resistor bank $R0$ is used for gain control, and a common-mode feedback (CMFB) circuit is implemented to set the operation point of the output node for large output swing. Another potential solution to address the gain limit of VGA is to use a N -path notch filter [52], which eliminates the even-order harmonics. However, more attention needs to be paid for extra filtering of up-converted harmonics if this scheme is to be used.

D. Harmonic-Rejection Lock-In Detector

Conventional lock-in detectors without harmonic rejection [53], [54] suffer from the interference and noise folding at the unwanted harmonics of the reference clock f_{ref} , which degrades the clock stability. Fig. 10 shows the schematic and phasor diagram of a classic third- and fifth-order harmonic-rejection schemes [55], which utilizes switches driven by a quadrature-phase clock and ratioed transconductance g_m to eliminate the third- and fifth-order harmonics of f_{ref} . g_m is provided by the MOS transistors biased at saturation region. However, these biased transistors exhibit excessive flicker noise, which cannot be well suppressed due to the limited

VGA gain in our CSMC architecture. To solve this issue, an HRLKD is innovated, as shown in Fig. 10(b). It replaces the g_m cells with a set of ratioed resistors ($R:R/\sqrt{2}:R$). Similar to the conventional scheme in Fig. 10(b), at the V_{out} node, the currents in the three paths recombine constructively when $f_{in} = f_{ref}$ and cancel at $f_{in} = 3f_{ref}$ and $f_{in} = 5f_{ref}$. The output capacitor C performs additional low-pass filtering. Since resistors and MOS switches exhibit near-zero flicker noise, the proposed HRLKD is better suited for our CSMC. Fig. 11(a) presents a detailed schematic of the HRLKD. The input of HRLKD is buffered with a source follower for its low output impedance. Meanwhile, differential signaling is used to suppress unwanted even-order-harmonic responses too. The quadrature clock ($f_{ref} = 4 \cdot N \cdot f_m$) of HRLKD is obtained from the reference clock generated in the WM described previously [see Fig. 8(a)]. By specifying the harmonic index N , the CSMC can lock to the desired N th-order dispersion curve. The simulated harmonic-rejection ratio in Fig. 11(b) is > 80 dB for the second- to sixth-order harmonics. The simulated output noise floor is shown in Fig. 11(c). Note that the flicker noise of the source follower is upconverted and is not translated into the output of HRLKD. The current noise floor near dc is dominated by the noise of output resistance R_{out} of HRLKD. Since the ratioed resistors inside the HRLKD adopt R of 100 k Ω , the output resistance R_{out} is 37 k Ω . Next, we note that the output dc offset voltage of the HRLKD also induces clock drift, with a relative clock frequency dependence of $5.0 \times 10^{-11}/\mu\text{V}$ in our simulation. Due to the 50% duty cycle of the HRLKD clock, the measured output dc offset voltage is lower than 10 μV , and its low sensitivity to temperature causes negligible clock instability. Finally, we note that the output resistance of HRLKD and the input capacitance of GDC [see Fig. 11(a)] determine the dominant pole of the CSMC feedback control loop. A low dominant pole is achieved by using the Miller capacitor C_2 in GDC.

E. Chip-Integrated Slot-Array-Based THz Waveguide Coupler

Low-loss chip-to-molecular cell interface is critical to maintain optimal systematic SNR and avoid the need for high THz power generation in the CSMC. Prior waveguide E -plane quartz probes [49] and dielectric-resonator-based couplers [56] rely on off-chip components for THz-wave coupling. They present high insertion loss, high assembly cost, and also large sample-to-sample variation. On-chip integrated dipole coupler was demonstrated [57], but it requires not only wafer thinning to tens of μm but also through-chip vias to suppress the substrate mode, which is not available in many CMOS processes. In this work, a pair of slot array couplers are innovated as the chip-to-molecular cell interface. Its 3-D structure is shown in Fig. 12(a), where four double-slot radiators fed by a slot balun [48] radiate downward into the un-thinned silicon substrate ($T = 304.8$ μm). The WR-4.3 metal waveguide opening (1.092×0.546 mm^2) is attached directly to the backside of the CMOS chip. With optimal slot array dimension, electromagnetic mode matching between the chip-launched fields at the silicon-air interface and the TE_{10} mode in the metal waveguide is achieved and enables efficient coupling.

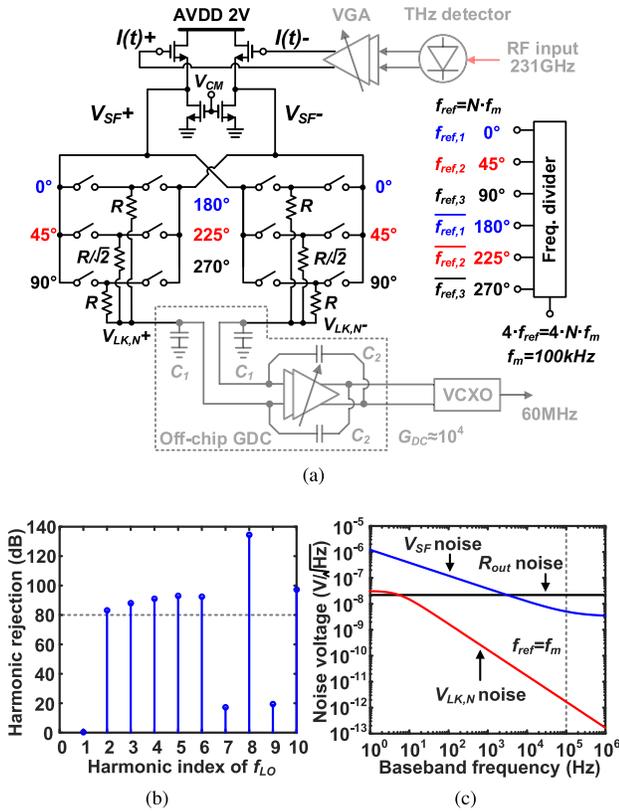


Fig. 11. HRLKD. (a) Detailed schematic. (b) Simulated harmonic-rejection ratio with $f_{ref} = 100$ kHz. (c) Output noise floor of the HRLKD output $V_{LK,N}$ versus the noise floor of source follower V_{SF} and the thermal noise of output resistance R_{out} .

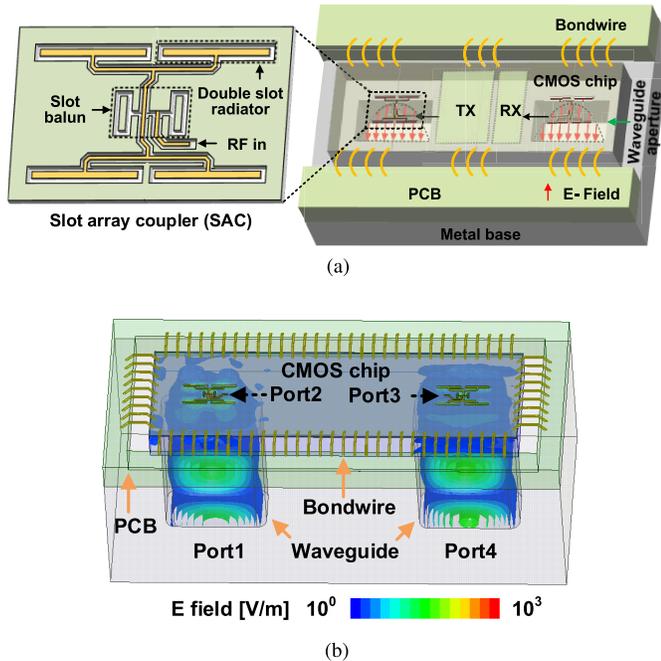


Fig. 12. Slot array couplers. (a) 3-D structure and (b) simulated electrical-field distribution at 231 GHz.

Fig. 12(b) shows the simulated electrical-field distribution of the slot array coupler pair. Port 1 and Port 4 are WR-4.3 waveguides with the TE₁₀ mode. Port 2 and Port 3 are on-chip shielded microstrip line with quasi-TEM mode. The

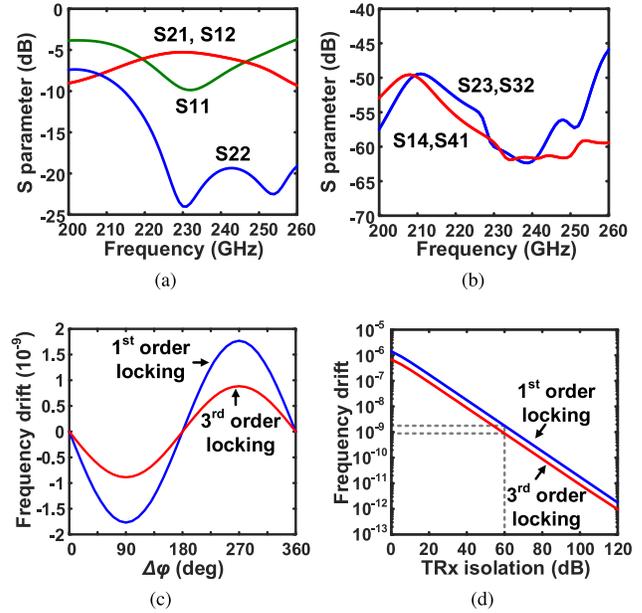


Fig. 13. Simulation results of slot array coupler. (a) Transmission and reflection losses. (b) Tx-Rx isolation. (c) Frequency drift at varying $\Delta\phi$ (with -60 -dB Tx-Rx isolation). (d) Frequency drift at varying isolation levels (with $\Delta\phi = 90^\circ$ or 270°).

launched waves are concentrated in the substrate, rather than the front side of the chip, due to the high permittivity of silicon. As a result, the slot array coupler is insensitive to the bond wires and external components on the PCB. A minimum of 5.2-dB transmission loss and a 21% fractional 3-dB bandwidth are obtained in the simulation, as shown in Fig. 13(a). A 5-dB loss reduction is achieved compared with that in [34], resulting in ~ 20 -dB system SNR improvement. The loss can be further reduced by ~ 3 dB if the resistivity of the silicon substrate is increased as the cases of, for instance, CMOS SOI processes [58].

It is noteworthy that an undesired clock drift can be generated by any Tx-to-Rx leakage through the substrate; it is sensitive to the phase difference $\Delta\phi$ between the above leakage signal and the normal transmitted signal through the gas cell [see Fig. 13(c)]. Since $\Delta\phi$ can be affected by the thermal contraction/expansion of the gas cell, the above Tx-to-Rx leakage should be minimized. In our work, that is achieved by the endfire nulling of the 2×2 array configuration [see Fig. 12(a)]. As shown in Fig. 13(b), excellent Tx-to-Rx isolation of 60 dB is obtained in the simulation. In the worst case [90° or 270° phase difference in Fig. 13(c)], the 60-dB isolation leads to a frequency drift of 1.8×10^{-9} for the first-order locking and 0.9×10^{-9} for the third-order locking [see Fig. 13(d)]. In the future, even higher isolation in CSMC may be achieved by an active cancellation technique [59]. Since the presented slot-array coupler requires no off-chip component nor wafer thinning, the clock packaging is significantly simplified (more details given in Section V-A).

V. EXPERIMENTAL RESULTS

A. Chip Packaging With Molecular Gas Cell

The chip is fabricated using TSMC 65-nm bulk CMOS technology. The die photograph is shown in Fig. 14. The chip has a

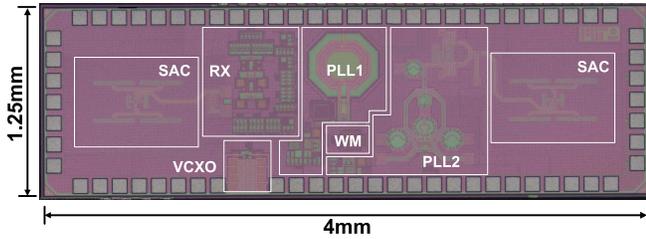


Fig. 14. Die photograph of the CMOS molecular clock chip.

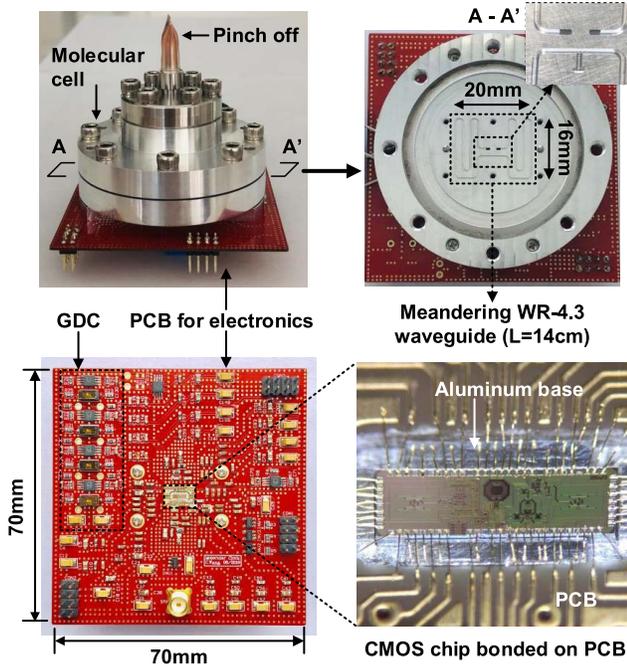


Fig. 15. Packaging of a CSMC module. (a) Gas cell and CMOS chip bonded on PCB. (b) Hermetically sealed gas cell with optically transparent epoxy.

dimension of $4 \times 1.25 \text{ mm}^2$ and an un-thinned ($305 \text{ }\mu\text{m}$), low-resistivity ($10 \text{ }\Omega\text{-cm}^{-1}$) silicon substrate. The packaged CSMC module is shown in Fig. 15(a). It contains an aluminum molecular cell fabricated via computerized numerical control (CNC) milling. The meandering WR-4.3 waveguide has an optimum length of 14 cm for the highest SNR [48]. As shown in Fig. 15(b), the two WR4.3 waveguide apertures of the gas cell are sealed by the optically transparent epoxy EPO-TEK 301-2 [60]. To avoid gas leakage and outgassing, the molecular cell

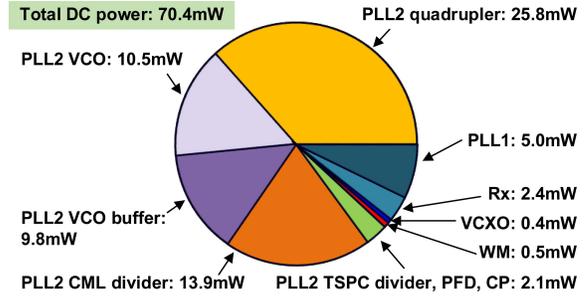


Fig. 16. DC power consumption breakdown.

TABLE I
PARAMETERS OF THE MEASURED ODD-ORDER DISPERSION CURVES

	1 st -order	3 rd -order	5 th -order
SNR (dB)	83.5	65.7	58.8
Amplitude*, V_{amp} (mV)	165.0	63.8	26.7
Offset voltage, V_{offset} (mV)	1.1	0.0043	0.0012
V_{amp}/V_{offset}	150.0	14844	22250

*The amplitude refers to half of the peak-to-peak voltage in Fig. 18.

is first evacuated to high vacuum through the OCS inlet/outlet with a cutoff frequency much higher than the probing signal to prevent the signal leakage. Next, the standalone gas cell without the CMOS chip is baked under a temperature of $150 \text{ }^\circ\text{C}$ for 72 h. Then, OCS molecules are injected with a pressure of 10 P. Finally, a copper tube connecting the molecular cell with the vacuum system is pinched-off, so as to realize a standalone molecular cell with hermetic sealing [see Fig. 15(a)]. The CMOS chip is glued on top of the aluminum base with two waveguide openings of the molecular cell. The special mechanical structure on the aluminum base ensures an alignment tolerance of $\pm 20 \text{ }\mu\text{m}$. Then, the CMOS chip is wire-bonded to a PCB with other periphery circuits (e.g., GDC and the bias circuits). We emphasize that the current packaging is not optimized for the minimum form factor. The ultimate limiting factor of the CSMC size is the THz waveguide itself, which has a volume of $20 \times 16 \times 1.1 \text{ mm}^3$. With micromachined THz waveguide technologies in the substrate, such as silicon [61], low-cost CSMC with a size of 1 cm^3 is feasible. The CSMC chip consumes a total dc power of 70.4 mW, of which a breakdown is given in Fig. 16. Out of that, $\sim 88\%$ (i.e., 62 mW) is from the PLL2 used for THz power generation. We see a decent room for dc power reduction. For instance, as described in Section IV-E, the generated probing power can be cut by $\sim 2 \times$ if a high-resistivity silicon substrate is used.

B. Electrical-Performance Characterization of the Chip

The THz output power of the clock module is measured by connecting its WR-4.3 waveguide interface with an Erickson PM-5 power meter. As shown in Fig. 17(a), the peak output power, including the loss of slot-array coupler (5.2 dB in simulation), is -9.4 dBm at 231 GHz. The output has a 3-dB bandwidth of 22 GHz (9.5%) and a PLL locking range of 26 GHz (11.3%). The measured output power agrees well with

TABLE II
COMPARISON TABLE OF HIGH-STABILITY, MINIATURIZED CLOCKS

Parameters	SiTime [12]	Microsemi [19]	JSSC2019 [23]	JSSC2018 [34]	This work
Clock Mechanism	OCXO	^{133}Cs CSAC	^{133}Cs CSAC	$^{16}\text{O}^{12}\text{C}^{32}\text{S}$ CSMC	$^{16}\text{O}^{12}\text{C}^{32}\text{S}$ CSMC
Timebase Frequency (GHz)	0.06	4.6	4.6	231.061	231.061
ADEV σ_y ($\tau = 10^0$ s)	3.0×10^{-11}	3.0×10^{-10}	8.4×10^{-11}	2.4×10^{-9}	3.2×10^{-10}
ADEV σ_y ($\tau = 10^3$ s)	4.0×10^{-11}	1.0×10^{-11}	0.8×10^{-11}	3.8×10^{-10}	4.3×10^{-11}
Temperature-Induced Drift [†]	$\pm 5.0 \times 10^{-9} \dagger\dagger$	$\pm 5.0 \times 10^{-10} \dagger\dagger$	$\pm 1.0 \times 10^{-9} \dagger\dagger$	N/A	$\pm 3.0 \times 10^{-9} \dagger\dagger$ or $\pm 5.0 \times 10^{-8} \dagger\dagger\dagger$
Magnetic Sensitivity (Gauss ⁻¹)	N/A	$\pm 9.0 \times 10^{-11}$ ‡	N/A	N/A	$\pm 2.9 \times 10^{-12}$ ‡‡
Start-up time (s)	120	180	N/A	< 1	< 1
DC power (mW)	600	120	60	66	70

[†] Temperature range in the measurements: $-20 \sim +70^\circ\text{C}$ for [12], $-10 \sim +70^\circ\text{C}$ for [19], [20], $+27 \sim +65^\circ\text{C}$ for this work

^{††} With temperature compensation ^{†††} Without temperature compensation.

[‡] The CSAC in [19] and [20] are equipped with dedicated magnetic shield, whereas this CSMC is directly exposed to the magnetic shield.

^{‡‡} The magnetic sensitivity is estimated based on the measured drift at 75 Gauss and on a simplified linear dependency assumption.

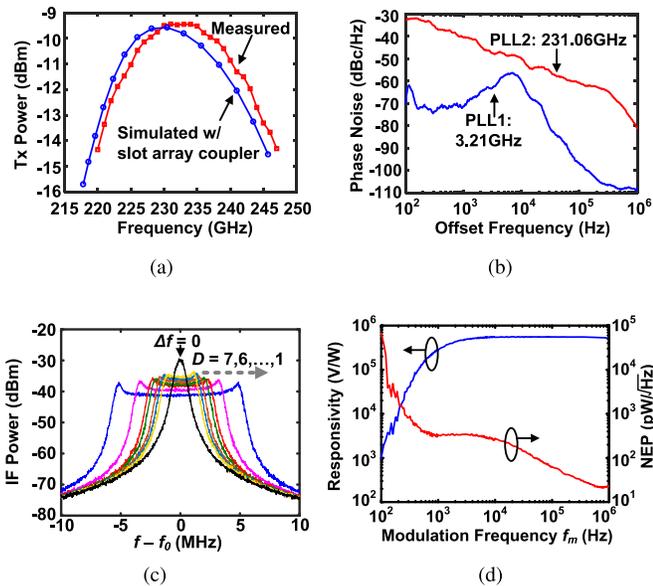


Fig. 17. Measurement results of the spectroscopic Tx and Rx. (a) Measured output RF power versus the simulated RF power, including the loss of slot array coupler. (b) Phase noise of first-stage PLL at 3.21 GHz and second-stage PLL at 231.061 GHz without modulation. (c) Spectrum of THz probing signal with modulation. Different Δf 's are applied by specifying the attenuator code D in WM. $f_0 = 231.061$ GHz. (d) Responsivity and NEP of Rx at 231 GHz.

the simulated results, which proves the effectiveness of the slot-array coupler. Next, the phase noise of the 3.21-GHz PLL1 output signal, measured by a Keysight N9020A spectrum analyzer, is -96.7 dBc/Hz at 100-kHz offset frequency and -107.5 dBc/Hz at 1-MHz offset frequency [see Fig. 17(b)]. The phase noise of the 231.061-GHz PLL2 output, measured through a VDI even-harmonic mixer, is -60.7 dBc/Hz at a 100-kHz frequency offset and -81.5 dBc/Hz at a 1-MHz frequency offset. This is comparable with the THz sources using coupled oscillator arrays [62], [63] that consume $10\times$ higher dc power. Nevertheless, the associated SNR limit due to a PM-to-AM noise conversion of the spectral line absorption [48] is estimated to be 84 dB. This is currently a major limiting factor of the clock medium-term stability, which

will be further discussed in Section V-C. At 231.061 GHz, the measured phase noise is only 2 ~ 3 dB worse than the simulation: -62.3 dBc/Hz at a 100-kHz frequency offset and -84.9 dBc/Hz at a 1-MHz frequency offset. Note that the simulation includes the VCO noise, the thermal noise of gate bias [V_{gg} in Fig. 7(a)], and the AM-to-PM noise conversion due to non-linearity of 231-GHz quadrupler but excludes the power supply noise. Hence, the off-chip power supply noise is one factor that may degrade the PLL performance. As a reference, in this work, Tektronix PWS 4323 with on-board capacitor array is used to power the chip. Next, after enabling the wavelength modulation, the output spectrum of the probing signal with different Δf 's is shown in Fig. 17(c). Δf is adjusted through the digital attenuator in Fig. 8.

Finally, the Rx performance is characterized by an external VDI THz source with a tunable f_m and a Stanford Research System SR865A lock-in amplifier. At $f_m = 100$ kHz, the measured responsivity and NEP achieve 5.5×10^5 V/W and 62.8 pW/ $\sqrt{\text{Hz}}$, respectively. An NEP of 19.0 pW/ $\sqrt{\text{Hz}}$ is derived after de-embedding the loss of the slot array coupler, and such performance is similar to state-of-the-art silicon-based THz detectors [64].

C. Characterization of the Clock System

The CSMC under an open-loop configuration is used as a spectrometer to measure the first-to-fifth order dispersion curves. In this configuration, the on-chip Tx and Rx are enabled. A Tx probing signal with $f_m = 100$ kHz and $\Delta f = 2.5$ MHz probes the spectral line in the molecular cell. The frequency deviation $\Delta f = 2.5$ MHz is selected experimentally with the highest SNR $\times Q$ product, which is higher than $\Delta f = 1.25$ MHz in Fig. 4 due to the broadening of power saturation effect [37]. By sweeping the PLL frequency, the multi-order dispersion curves are demodulated by the HRLKD, as shown in Fig. 18. Table I summarizes the measured dispersion curve parameters. For the first-order dispersion curve, an SNR of 83.5 dB is obtained. Compared with [34], a 10.8-dB higher RF probing power is achieved by employing the low loss slot array coupler and an improved Tx design. In addition,

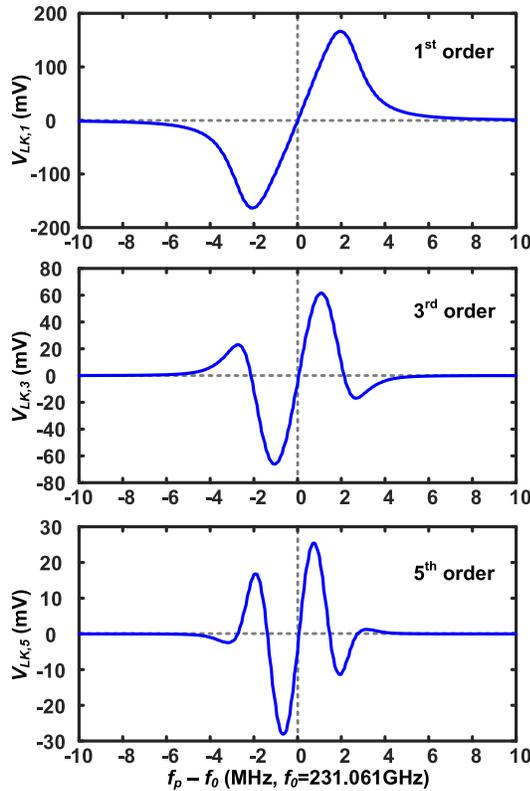


Fig. 18. Measured odd-order dispersion curves under an open loop configuration of CSMC. The measurement setup: $f_m = 100$ kHz and $\Delta f = 2.5$ MHz ($D = 3$). $V_{LK,N}$ are the dc output voltages of HRLKD.

due to a lower flicker noise enabled by a faster modulation frequency f_m , the low loss slot array coupler, and an optimized square-law detector, the Rx reduces the NEP by $8\times$. Hence, a 39.6-dB SNR enhancement is expected (if the saturation effect is ignored). However, the measurement only presents a 30.5 dB higher SNR (from 53 dB in [34] to 83.5 dB in Table I). As shown in Section V-B, the SNR limited by the Tx phase noise through PM-to-AM noise conversion is 84 dB, which is close to the 83.5-dB system SNR. Thus, the Tx phase noise, instead of the link budget, determines the threshold of SNR in the current system. In addition, it can be clearly seen that the SNR and the amplitude V_{amp} decrease in higher order dispersion curves. This degradation comes from: 1) the high-order derivative of the line profile and 2) the frequency pulling of PLL, as mentioned in Section IV-A. In addition, as expected, the third- and fifth-order dispersion curves present much lower offset voltage V_{offset} . Even after normalizing V_{offset} with the different V_{amp} 's, the third- and fifth-order curves are still two orders of magnitude better than the first-order curve. It verifies the effectiveness of high-order probing in dealing with the transmission-baseline tilting. Considering a tradeoff between the SNR and the offset voltage V_{offset} , the third-order dispersion curve is selected for the closed-loop CSMC.

The setup and the measured Allan deviation of the closed-loop third-order CSMC are shown in Fig. 19. The Allan deviation is measured by a Keysight 53230A frequency counter referenced to a 10-MHz Stanford Research System Rubidium

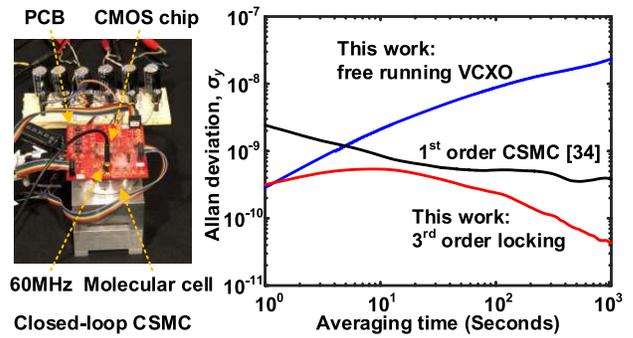


Fig. 19. Photograph of the closed-loop CSMC setup and the measured Allan deviation.

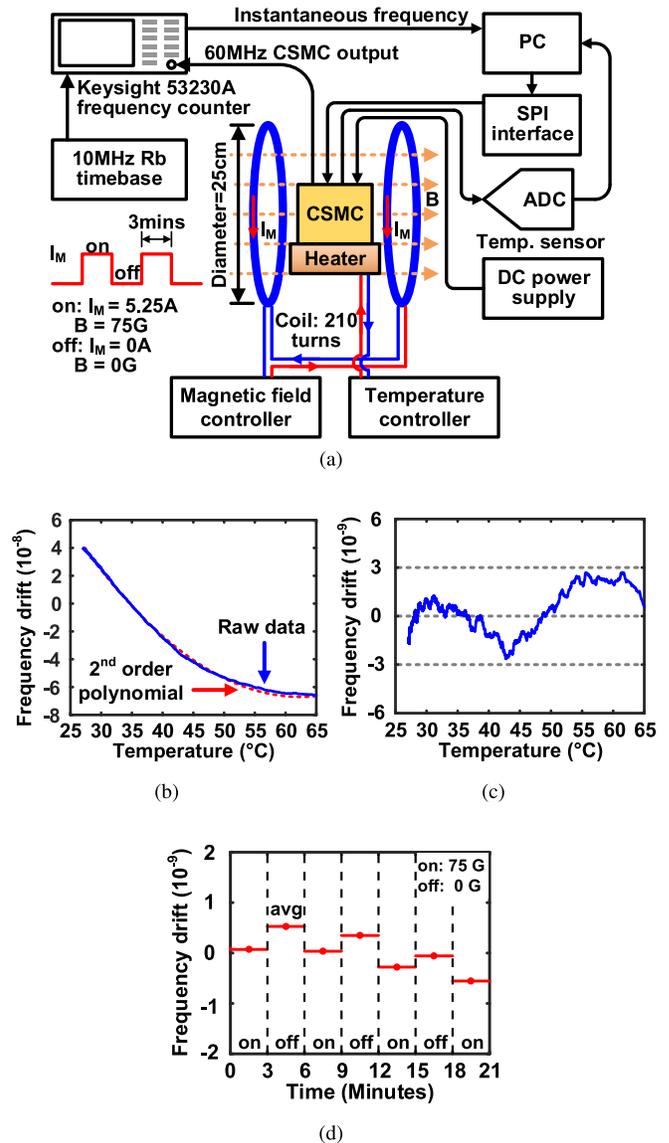


Fig. 20. Sensitivity of the clock to environmental disturbances. (a) Measurement setup. (b) Raw data of temperature induced frequency drift. (c) Temperature dependence with the second-order polynomial compensation. (d) Frequency drift under a strong, externally applied magnetic field of 75 G.

atomic clock (PRS10). With a unity gain loop bandwidth of 5.5 mHz, the third-order CSMC exhibits an Allan deviation of 3.2×10^{-10} for an averaging time of $\tau = 1$ s and

4.3×10^{-11} for an averaging time of $\tau = 10^3$ s. Compared with the free-running VCXO, the medium-/long-term stability at $\tau = 10^3$ s is improved by almost three orders of magnitude. Fig. 20(a) shows the measurement setup for the clock temperature dependence and the magnetic field sensitivity. The temperature is controlled by a heater beneath the CSMC. Without any temperature compensation, the CSMC frequency drifts by $\pm 5 \times 10^{-8}$ over a temperature range of 27°C – 65°C [see Fig. 20(b)]. With an on-chip temperature sensor (see Fig. 5) and a simple second-order polynomial compensation, the clock drift is reduced to $\pm 3 \times 10^{-9}$, as shown in Fig. 20(c). It should be noted that the current temperature measurement range is limited by the test setup and the ability to dynamically adjust the bias current (especially for the CML divider in Fig. 6) to maintain the clock locking. Assuming that these technical issues can be solved in the future, it is expected that the compensated frequency over the full temperature range (-10°C – 70°C) should be comparable to the presented value. Furthermore, note that the frequency stability shown in Fig. 19 has no temperature compensation. A long-term stability measurement with up to $\tau = 10^4$ s has also been conducted, with an Allan deviation result of 8.8×10^{-11} using the second-order polynomial compensation similar to that in Fig. 20(b). With our ongoing improvement of the gas cell quality and development of clock architectures with built-in real-time compensation, performance at even longer term (e.g., $\tau = 10^5$ s) will be investigated in the future.

Finally, it is noteworthy that the CSMC is by principle insensitive to external magnetic field variation [35] because the rotational spectral lines only respond to the second-order Zeeman shift, and its gyromagnetic factor (i.e., g -factor) is much lower than that in CSACs. To verify this, a 75-G magnetic field is applied every other 3 min via a custom-made Helmholtz coil [see Fig. 20(a)]. As shown in Fig. 20(d), a corresponding frequency fluctuation of $\sim 4 \times 10^{-10}$ is observed from the CSMC. That is equivalent to a very low magnetic-field sensitivity of $\pm 2.9 \times 10^{-12} \text{ G}^{-1}$.

VI. CONCLUSION

The transmission baseline tilting is a key issue that results in the medium-/long-term frequency drift of CSMCs. In this work, a high-odd-order CSMC on 65-nm CMOS technology is innovated. It effectively reduces the impact of the transmission baseline tilting by locking to a high-odd-order dispersion curve of wavelength-modulation spectroscopy. Table II compares the high-order CSMC with other high-stability, miniaturized clocks. Firstly, the all-electronic CSMC marks a dramatic cost reduction compared with CSACs due to its CMOS chip core and simplified package. Next, with an improved spectroscopic system and high-order locking scheme, the clock stability at $\tau = 1$ s and $\tau = 10^3$ s is improved by $8\times$ and $9\times$, respectively, comparing to the first CSMC prototype [34]. In addition, the excellent temperature stability of $\pm 3 \times 10^{-9}$ is achieved without using oven-controlled temperature stabilization. Furthermore, without any magnetic shield, the magnetic field sensitivity of the high-order CSMC is $30\times$ less than the state-of-the-art CSACs with dedicated shields. Also, note that

CSMCs have faster startup time because there is no Alkali evaporation and temperature stabilization as those in CSACs are needed. Finally, competitive 70.4-mW power consumption of the presented CSMC makes it suitable for power-constraint applications. It should be noted that, as an emerging technology, the CSMCs still have vast room for performance and efficiency improvement. That is particularly justified with the recent advances in CMOS processes, which now offers transistors with f_{max} around 400 GHz [65], [66]. Therefore, a CSMC with atomic-clock-grade stability, cm^3 volume, and $<50\text{-mW}$ dc power becomes feasible in the near future.

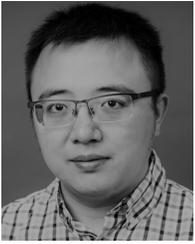
ACKNOWLEDGMENT

The authors appreciate the help of Dr. Stephen Coy, Prof. Robert Field, and Prof. Keith Nelson from the Department of Chemistry, Massachusetts Institute of Technology (MIT), Prof. John Muentner from the Department of Chemistry, University of Rochester, and Dr. Bradford Perkins from MIT Lincoln Laboratories. They also acknowledge the technical discussions with Dr. Dennis Bus and Dr. Juan Herbsommer at the Texas Instruments Kilby Laboratory, Prof. Hae-Seung Lee at MIT, Dr. Lin Yi at the NASA Jet Propulsion Laboratory, and Dr. Cort Johnson at the Draper Laboratory.

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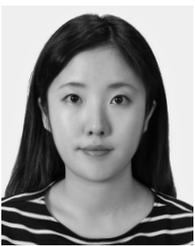
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