11.9: A 105 Gb/s Dielectric-Waveguide Link in 130nm BiCMOS Using Channelized 220-to-335GHz Signal and Integrated Waveguide Coupler

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\textsuperscript{3}Intel, Chandler, AZ
Self Introduction

- S.B. Mathematics, S.B. Electrical Engineering MIT
- M.Eng. Electrical Engineering & Computer Science MIT
- Ph.D. Electrical Engineering MIT
- United States Marine Corps 2006 – 2019
- Office of Naval Research 2014 – 2017
- MIT Lincoln Laboratory 2015 – 2018
- Naval Research Laboratory 2014 – 2020
- Raytheon Technologies 2018 – Present

Interests
- High-performance RF/mixed signal microelectronics
- Heterogenous integration/packaging
- Analog signal processing
- Microwave photonics
Outline

- Introduction
- Architecture
- Circuit Description
- Experimental Results
- Conclusion
Introduction: Application

- Intermediate range (~1m)
- High-rate (100+ Gbps)
- Monolithic
- Simple packaging
- Energy-efficient (~pJ/bit)
- Throughput density (300+ Gbps/mm)
Introduction: Application

Backplane Package-Package Interconnect

- Better energy efficiency than photonics or copper in meter-class links
- High data rates over .1-1m
- Large throughput density
- Low-cost integration/packaging
Introduction: Application

Backplane-Backplane Fly-Over Cable Concept

- The waveguide flexibility
- Small cross section
- Efficient operation over ~1m
Key Enabler: Sub-THz Dielectric Waveguides

Channel Loss, 1 Meter

Sub-THz Dielectric Waveguide Est. Loss

Dielectric Waveguides

1m Twinax

Channel Bandwidth (GHz)

$S_{21} (\text{dB})$

[0 5 10 15 20 25 30]

-30 -25 -20 -15 -10 -5 0

Sub-THz Dielectric Waveguide Est. Loss

400 μm

Waveguide Bond Surface Contour

$E_{11}^{x}$

235 GHz 275 GHz 315 GHz

Field Strength $E_{11}$

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J. Holloway et al., IEDM, 2020
Comparison

- 57 GHz and 80 GHz duplex operation
- Single-channel scheme
- Off-chip coupler
- Planar coupler/waveguide architecture

**Demonstration:**
- Data rate: 12.5 Gbps, full-duplex (25 Gbps)
- Link efficiency: 5.7 pJ/bit
Comparison

- 130 GHz operation
- Single-channel scheme
- Off-chip coupler
- Planar coupler/waveguide architecture

Demonstration:
- Data rate: 36 Gbps
- Link efficiency: 6 pJ/bit (transmitter only)

[M. Sawaby et al., SSC-L, 2018]

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Comparison

- 140 GHz operation
- Single-channel scheme
- Off-chip coupler
- Orthogonal coupler/waveguide scheme

Demonstration:
- Data rate: 12 Gbps
- Link efficiency: 19.2 pJ/bit

[M. De Wit et al., ESSCIRC, 2016]
Comparison with Dielectric Waveguide Links

- Electrical links provide high efficiency below 56 Gbps
  - Dielectric links must maintain competitive efficiency and show data rate scaling beyond 100 Gbps to be competitive
Comparison with Dielectric Waveguide Links

- Research focus on planar monolithic/in-package links
- Multiple sub-THz channels to maximize available guide bandwidth
- Higher frequency operation to improve bandwidth and reduce size
Outline

- Introduction
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Architecture Concept

- On-chip sub-THz carrier generation
Architecture Concept

• Baseband bit streams modulate each carrier
Architecture Concept

- A sub-THz multiplexer combines channels

Sub-THz Source

Freq. Synth. & Baseband Control

Baseband Data 1 (BD1)

BD 2

BD 3

Transmit Data Stream

Digital Block

220-335 GHz Multiplexer

220 260 300 GHz

35GHz 5GHz

fC1 fC2 fC3
Architecture Concept

- Power coupled to- and transported along low-loss dielectric waveguides
Architecture Concept

- Independent channels separated and demodulated on receive
Link Demonstration

- Designed and implemented in IHP 130 nm BiCMOS process
  - SG13G2, $f_t = 300$ GHz, $f_{max} = 500$ GHZ HBT
- Three-channel transmitter, single-channel receiver for testing
Transmitter Architecture

- Single-chip generates three sub-harmonic carriers
- System performs harmonic doubling and modulation
- On-chip multiplexer channelizes/aggregates RF spectra
- Broadband coupler launches the sub-THz energy
Outline

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Link Transmitter Chip: Amp. Multiplier Chain

- Off-chip V-band source
- Multiplied and amplified to generate a 130 GHz seed carrier
Link Transmitter Chip: AMC

- Nominal 0 dBm input power, 3.2 dBm output power
- 45 dBc spur performance
- Approx. 8 GHz input LO BW: 48 GHz sub-THz BW
Link Transmitter Chip: 5dB Coupler

- A two-stage 3-way Wilkinson divider-based 5dB coupling
  - Provides ~5.4 – 5.8 dB coupling
  - Less than 0.1dB asymmetry across 110-150 GHz
Link Transmitter Chip: SSB Mixers

- A quadrature SSB mixer generates 110 GHz and 150 GHz carriers
- Single mixer core, up/down conversion via $V_A - V_D$ phase reordering
Link Transmitter Chip: SSB Mixers + PAs

- Tuned PA2 amplifiers provide an additional sideband suppression and gain
- Simulated output power: -2.3 dBm to -0.4 dBm
Link Transmitter Chip: Doubler-Modulator

- A combined doubler-modulator provides modulated power
Link Transmitter Chip: Doubler-Modulator

- Single broadband stop provides high impedance across band
Link Transmitter Chip: Doubler-Modulator

- Simulated upper sideband modulation power: -14 dBm to -9.5 dBm
Sub-THz Channelizers

• Channelizer performance impacts receiver SINR
  – Directly impacts link efficiency, capacity, and bit error rate (BER)
• Channel fractional bandwidth and filter roll-off drive higher-order conventional filters
  – Lower on-chip passive quality factor at sub-THz worsens insertion loss
On-Chip Channelizers: Channel Filters

- Quarter-wave microstrip tuned to maximize individual resonator $Q_u$
- Mixed electric & magnetic coupling used to realize filter response
On-Chip Channelizers

- Excellent agreement between simulation and measurements
Integrated Sub-THz Coupler

- Tapered, enclosed structure, differentially driven
- Guide mode matched to slot-line leaky mode

Waveguide Hybrid Mode Profile

Dielectric Waveguide

BEOL Coupler Structure

Guided Mode

Vin

315 GHz

235 GHz

[J. Holloway et al., T-MTT, 2017]
Integrated Sub-THz Coupler

- Wideband single-ended to differential transition
- Direct waveguide bonding
Link Receiver Chip

- Single-channel receiver chip
Link Receiver Chip

- Single-channel receiver chip
- Gilbert switching quad provides down-conversion
  - Tail transistors provide wideband differential current and match to coupler
  - Emitter followers provide voltage translation
Link Receiver Chip

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- Single-channel receiver chip
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  - Emitter followers provide voltage translation
- Wideband baseband amplifier pair drives off-chip measurements
Link Receiver Chip

- Simulation with full-wave interconnect demonstrates more than 30 GHz of receiver bandwidth in all channels
- Simulated DC power consumption:
  - 20 mW (mixer) + 45 mW (baseband amplifiers)
Outline

■ Introduction
■ Architecture
■ Circuit Description
■ Experimental Results
■ Conclusion
Link Transmitter Chip

- Measured 3.9 x 2.4 mm
- Consumes 256 mW
Link Receiver Chip

- The final circuit measures 0.9 mm x 0.9 mm and consume 73 mW
Power Measurement

- Waveguide power meter used to measure TX power in each channel
Power Measurement

- Waveguide power meter used to measure TX power in each channel
Power Measurement

- Waveguide power meter used to measure TX power in each channel
- Measured power agrees with the simulation
  – Waveguide – horn mode conversion not modeled
Link Testing: Setup

- Waveguide bonded to the chip surfaces
- Two wideband PRBS generators used to excite two adjacent channels at a time
Link Testing: Data Transmission

- Single-channel baseband measurements confirm PRBS spectrum
- Adjacent channel unmodulated carrier present
  - Attenuated by RX mixer and baseband amplifiers
Link Testing: Data Transmission

- Eye diagram measurements using uncorrelated adjacent channel PRBS data
- 35Gbps verified across all three channels
Link Testing: Data Transmission

- BER for two link lengths
- BER:
  - $< 5 \times 10^{-8}$ for 35Gbps, 30cm
  - $< 10^{-8}$ for 35Gbps, 5cm
- Eye closure from SNR, not from dispersion, ISI, or jitter

![Graph showing Bit Error Rate vs. Unit Interval for different channel lengths and channels.](image-url)
Adjacent Channel Interference

- Single 5cm link, 35Gbps
- Single-channel and two-channel operation
  - ~10x worse BER from adjacent channel interference
  - Remaining VSB power degrades SINR

[J. Holloway et al., Micro. Mag., 2020]
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**This Work**

- **Tech.**: 130nm BiCMOS
- **Carrier Freq. (GHz)**: 220, 260, & 300
- **Data Rate (Gbps)**: 35×3†, 5×10⁻⁸, 30×3†, <10⁻¹²
- **BER**: <10⁻¹²

| † Full-duplex transmission (12.5Gbps each direction) |
| † The link is demonstrated with a three-channel TX and one-channel RX |
| †† Input signal sources (16.25GHz in [2], 43.3, & 20GHz in this work) not included |
| ††† RX LO source (220~300 GHz) not included |

- Demonstration exceeds the aggregate data rate of the state of the art by approximately 3x at commensurate BER
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<sup>†</sup> Full-duplex transmission (12.5Gbps each direction)
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<sup>††</sup> RX LO source (220–300 GHz) not included

- Only published link incorporating a monolithically-integrated coupler

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• Smallest published waveguide cross section

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⁺ Full-duplex transmission (12.5Gbps each direction)
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‡ Input signal sources (16.25GHz in [2], 43.3, & 20GHz in this work) not included
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- Total link efficiency similar to lower-frequency implementation
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- **Almost 12x improvement in data rate density figure of merit**

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Conclusion

• Key passive device enablers demonstrated:
  – Multiplexers and couplers

• Successful demonstration of first:
  – Fully-monolithic,
  – Sub-THz dielectric,
  – Channel-aggregating link

• Competitive energy efficiency demonstrated in BiCMOS

• 3x improvement in lane capacity

• Approx. 12x improvement in lane capacity density
Acknowledgement

• Raytheon Technologies
• Intel Corporation
• Office of Naval Research (ONR)
• MIT Lincoln Laboratory
• Naval Research Laboratory (NRL)
• IHP
Thank you for your attention.