Realization of In-Band Full-Duplex Operation at 300 and 4.2 K Using Bilateral Single-Sideband Frequency Conversion

Xiang Yi, *Senior Member, IEEE*, Jinchen Wang, *Member, IEEE*, Marco Colangelo, *Graduate Student Member, IEEE*, Cheng Wang, *Member, IEEE*, Kenneth E. Kolodziej, *Member, IEEE*, and Ruonan Han, *Senior Member, IEEE*

***Abstract*— CMOS-integrated in-band full-duplex (IBFD) operation in wireless links and cryogenic quantum platforms was previously enabled by magnetic-free circulators using the phase non-reciprocity from spatial-temporal modulation. In this article, we present an alternative and simple integrated circuit scheme, which not only realizes non-reciprocal signal flows required for IBFD operations but also improves the isolation performance by completely eliminating any chip-level transmit (TX)-to-receive (RX) coupling. The above functions are enabled by performing a direction/frequency-independent, single-sideband down-conversion to the counter-propagating TX and RX signals, which creates opposite deviations of on-chip TX and RX frequencies with respect to the antenna (ANT) frequency. Such a principle also broadens the isolation bandwidth and enables integrated receiver down-mixing function. As a proof-of-concept, a 3.4–4.6-GHz (30% fractional bandwidth) IBFD interface is implemented using a 65-nm bulk CMOS technology. The measured TX-to-RX isolation of the circuit is 32–51 dB at 300 K, and 14–29 dB at 4.2 K. The measured TX-to-ANT and ANT-to-RX insertion losses are 3.0 and 3.2 dB at 300 K, and 1.9 and 2.0 dB at 4.2 K. At 300 K, the measured TX-to-ANT and ANT-to-RX IIP3 are 29.5 and 27.6 dBm, respectively. The IBFD core of the chip occupies an area of 0.27 mm^2 and has a dc power (nominally consumed in an on-chip modulation clock generator) of 48 mW at 300 K and 42.6 mW at 4.2 K.**

***Index Terms*— Bilateral frequency converter (BFC), coupling, cryo-CMOS, in-band full-duplex (IBFD), isolation, magnetic-free circulator, non-reciprocal, wideband.**

Manuscript received October 6, 2020; revised December 19, 2020 and February 11, 2021; accepted February 22, 2021. This article was approved by Associate Editor Mohyee Mikhemar. This work was supported by the United States Air Force under Contract FA8702-15-D-0001 through the Advanced Concepts Committee (ACC) fund at Massachusetts Institute of Technology (MIT) Lincoln Laboratory. *(Corresponding author: Ruonan Han.)*

Xiang Yi was with the Department of Electrical Engineering and Computer Science (EECS), MIT, Cambridge, MA 02139 USA. He is now with the School of Microelectronics, South China University of Technology, Guangzhou 510641, China, and also with the Pazhou Laboratory, Guangzhou 510663, China.

Jinchen Wang, Marco Colangelo, and Ruonan Han are with the Department of Electrical Engineering and Computer Science (EECS), MIT, Cambridge, MA 02139 USA (e-mail: ruonan@mit.edu).

Cheng Wang was with the Department of Electrical Engineering and Computer Science (EECS), MIT, Cambridge, MA 02139 USA. He is now with Analog Devices, Boston, MA 02110 USA.

Kenneth E. Kolodziej is with the MIT Lincoln Laboratory, Lexington, MA 02421 USA.

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3062079.

Digital Object Identifier 10.1109/JSSC.2021.3062079

I. Introduction

THE ever-increasing demands for wireless communication speed and sensing capability call for RF systems with more efficient utilization of the congested electromagnetic spectrum. Compared with conventional half-duplex modes, such as time-division duplex and frequency-division duplex, in-band full-duplex (IBFD) mode potentially doubles the utilization efficiency of the spectrum and simplifies the transmission protocols [1], [2]. Non-reciprocal electronic devices, such as isolator, gyrator, and circulator, are critical for full-duplex operations and have been extensively utilized in wireless data links and monostatic radars. In addition, a circulator capable of operating under cryogenic condition is critical in quantum computing platforms, in which a non-reciprocal path is needed to extract the weak qubit measurement signal while blocking any inverse disturbance from, for example, the pump signal of a parametric amplifier [3].

As shown in Fig. 1, a circulator is a three-port device that delivers signal to the next port in a certain rotation. It enables an IBFD system where the transmit (TX) and receive (RX) signals have identical frequencies on the chip and share a single antenna (ANT). Conventional ferrite circulators based on Faraday rotation are bulky and cannot be integrated on a chip. Recently, magnetic-free circulators have become attractive due to their compact size and compatibility with CMOS integrated circuit technologies [4]–[9]. Using time-variant devices, typically realized with clock-modulated switches in a N-path filter [2], such a component applies non-reciprocal phases to various signals at the same frequency; then, with another signal path through a delay line with reciprocal added phase, the circuit creates constructive addition to the desired signal at a certain port and cancellation to other undesired signals.

It is noteworthy that the TX-to-RX isolation is a key metric to all full-duplex systems. For example, a standard full-duplex wireless communication system requires >20-dB isolation at the RF interface [10], and a cryogenic circulator used for quantum computers typically provides a wideband >18-dB isolation [11]. However, a few imperfections may degrade the isolation. For example, the impedance mismatch at the ANT port causes part of the TX signal to be reflected to the RX port; this problem is normally alleviated by a post-fabrication/packaging impedance tuning at the ANT port.

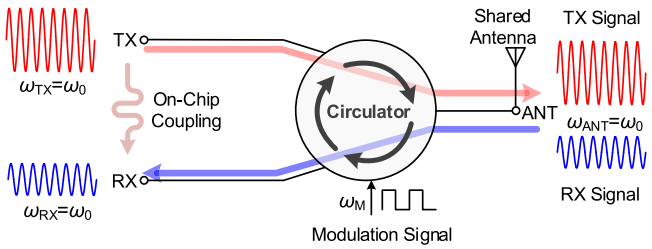


Fig. 1. Prior CMOS-circulator-based full-duplex interface: propagation and frequency allocation of the TX, RX, and ANT signals.

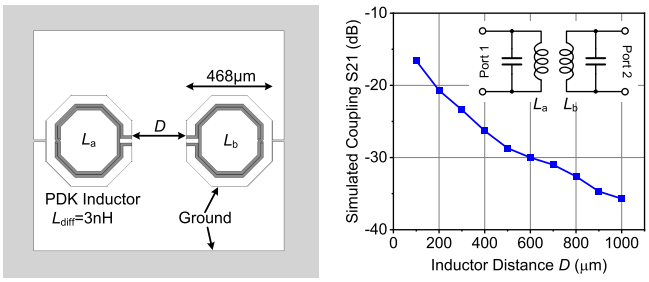


Fig. 2. Coupling between two standard inductors on a bulk CMOS substrate (10-$\Omega\cdot$cm resistivity) at 4 GHz. To mimic the normal application scenarios of inductors in radio frequency integrated circuits (RFICs), two capacitors (520 fF) are added to create resonance.

In the context of silicon integrated circuits, one critical limitation of isolation relates to the inevitable TX-to-RX coupling through the inter-inductor magnetic crosstalk doped silicon substrate (especially in bulk CMOS processes with typically 10-$\Omega\cdot$cm resistivity), on-chip power lines, and so on. In Fig. 2, a full-wave electromagnetic simulation shows that, on a silicon substrate with 10-$\Omega\cdot$cm resistivity, the coupling between two standard multi-coil inductors[1] at 4 GHz can be -20 dB or higher, when they are placed close to each other. Eight-shaped inductors effectively reduce the magnetic coupling but at the cost of degraded quality factor and much larger size [12]. It clearly indicates that a compact layout design poses significant challenges to an IBFD front-end circuit. Lastly, as described previously, the isolation of prior CMOS circulators relies on the cancellation of two precisely out-of-phase signals from two paths that are implemented with completely different manners. Correspondingly, the created isolation is narrowband in nature and is susceptible to non-ideal clocking and other amplitude/phase mismatches among the signal paths.

In this article, we present a fully integrated IBFD interface that utilizes a bilateral frequency converter (BFC) to realize non-reciprocity while addressing the above problems of CMOS circulators [13]. As shown in Fig. 3, the BFC is driven by a modulation signal ω_M and has two ports: one port is connected to the shared ANT, while the other port carries both the TX and RX signals. The key difference from a circulator (both standard and CMOS-based) is that, although the TX and RX frequencies are identical at the ANT interface (i.e., $\omega_{ANT}=\omega_0$), they are shifted to $\omega_0+\omega_M$ and $\omega_0-\omega_M$, respectively, inside the chip. The $2\omega_M$ separation is realized

[1]The simulation reflects a common scenario in an actual IBFD system that one of such inductors is used in a resonator circuit of the high-power TX chain, while the other inductor is used for the resonance in a sensitive RX chain.

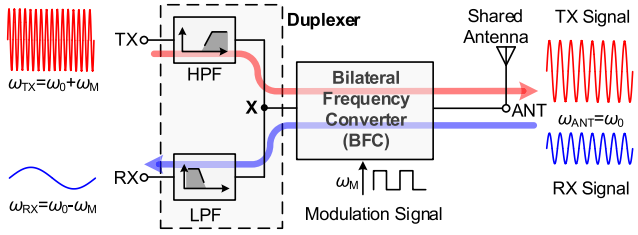


Fig. 3. Our BFC-based full-duplex systems: propagation and frequency allocation of the TX, RX, and ANT signals.

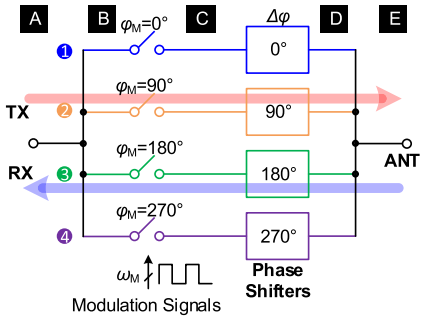


Fig. 4. Simplified schematic of the BFC.

through a *signal and direction independent downconversion process* in the BFC. The TX and RX signals can be then physically separated by a duplexer simply consisting of a high-pass filter (HPF) and a low-pass filter (LPF). Previouly in [14], such a frequency split was also realized through a modulated nonlinear transmission line. One clear advantage of the frequency split is that the aforementioned chip-level TX-to-RX coupling in a normal IBFD system is eliminated. Moreover, our analysis to be given in this article will also show that the TX-to-RX isolation of the circuit is wideband in nature and is robust against issues like device mismatch and non-ideal clocking.

As a proof-of-concept, a 4-GHz front-end that uses a standard 65-nm bulk CMOS technology is demonstrated and characterized at both 300 and 4.2 K. Effective isolation across $\sim$30% fractional bandwidth is obtained. This article is organized as follows. In Section II, a few key properties of a BFC are analyzed. Section III then presents the circuit implementation details of the 4-GHz IBFD interface. In Section IV, the measurement results are shown. Finally, a conclusion with a performance comparison with other CMOS circulators is given in Section V.

II. BFC With Irreversible Spectral Shift

The simplified schematic of a two-port BFC is shown in Fig. 4. It consists of four parallel paths, and each path is a series connection of one switch and one phase shifter. The switches are driven by modulation signals with quadrature phases, and they introduce frequency and phase shifts to signals flowing along the paths. Albeit the resemblance to a passive single-sideband (SSB) mixer, one important property of the presented topology that was unexplored before is its *irreversible* frequency conversion process, namely, the BFC always performs frequency downconversion regardless of the signal flow direction.

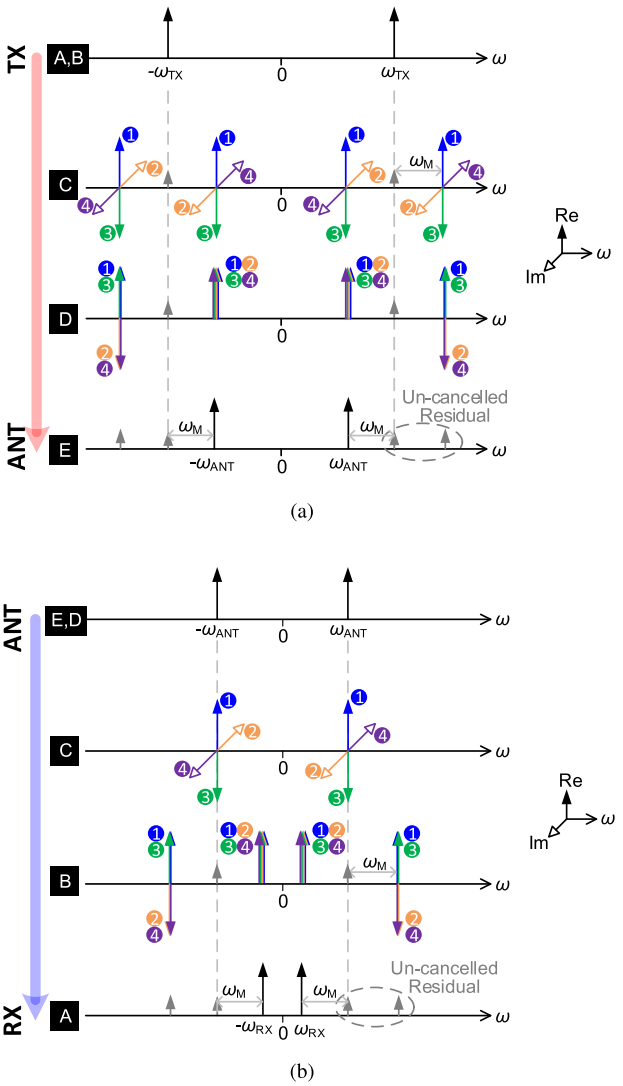


Fig. 5. Phasor diagrams of the signals flowing from (a) TX to ANT and (b) ANT to RX.

A. Irreversible Spectral Shift: Analysis

We examine the phasor diagram of signals at various stages (i.e., A∼E) of the schematic in Fig. 4.[2] Fig. 5(a) shows the signal flowing from TX to ANT. For simplicity, only the positive frequency components are described in the following. At Stage A and B, the TX signal at ω_{TX} is modulated with overlapping quadrature phases $\varphi_{\mathrm{M,\ i=1,2,3,4}}$ of 0°, 90°, 180°, and 270° in Path 1–4 of Fig. 4, respectively. Thus, at Stage C, the two generated sideband frequency components ($\omega_{\mathrm{TX}}-\omega_{\mathrm{M}}$ and $\omega_{\mathrm{TX}}+\omega_{\mathrm{M}}$) in Path i (i = 1, 2, 3, 4) carry the following phases:

$$\varphi_{\mathrm{C,\ i}} = \begin{cases} \varphi_{\mathrm{M,\ i}} & \text{for the upper sideband} \quad (1a) \\ -\varphi_{\mathrm{M,\ i}} & \text{for the lower sideband.} \quad (1b) \end{cases}$$

[2]For simplicity of the illustration, we assume that when a signal passes through a modulated switch, only the upper and lower sidebands remain, while the component at the original signal frequency vanishes. Strictly speaking, that is not true for the single-ended signaling in Fig. 4. But it does happen for the differential signaling in our actual design (Fig. 8).

Next, these signals flow through the phase shifters. The values of the applied phases are selected to compensate the phase differences of the lower sideband signals (i.e., $\Delta\varphi_{\mathrm{i}} = \varphi_{\mathrm{M,\ i}}$) among the four paths so that after the signal summation, only such lower sideband component is preserved at the ANT port. As a result, the TX signal is shifted down by ω_{M} when flowing to ANT.

For a signal flowing backward (i.e., ANT to RX), a similar phasor-diagram analysis can be applied. As shown in Fig. 5(b), again only the lower sideband signal ($\omega_{\mathrm{ANT}}-\omega_{\mathrm{M}}=\omega_{\mathrm{RX}}$) presents at Node A on the left. A key observation to straightforwardly explain such an irreversible frequency conversion is that the condition listed in (1) is always valid, regardless of the signal frequency and its flow direction through the switches. Similarly, the additional phase $\Delta\varphi$ applied by the phase shifters is also independent of the signal frequency and direction. The above two-step manipulation then always leads to the in-phase summation of the lower-sideband component and out-of-phase cancellation of the upper-sideband component, hence, an irreversible downconversion. As a result, the TX and RX signals have frequencies that are higher and lower than ω_{ANT} by ω_{M}, respectively. and are then readily diverted to two separate on-chip paths using an HPF for the TX port and an LPF for the RX port. Although the presented scheme does not deliver the exactly same functions as a conventional circulator, it still enables IBFD operation in light of the identical TX and RX frequencies at a shared ANT interface; meanwhile, the TX/RX frequency split eliminates any coupling between the TX and RX blocks on the same die.

B. Non-Reciprocity of the BFC

Although the overall circuit shown in Fig. 3 possesses a circulator-like behavior, up till this point, whether the BFC itself is non-reciprocal is not clear yet, especially considering that it supports signal flows in both the forward (i.e., left to right) and backward directions. It is noteworthy that prior studies and definitions of electrical reciprocity are all based on the assumption that all signals share an identical frequency [15]. That, however, makes the reciprocity analysis of the BFC, which involves frequency conversion, difficult. In [16], an approach using cross-frequency S-parameters is used to model a frequency mixer, but such S-parameters cannot directly provide the reciprocity property of a system.

In this section, we present an alternative approach that mathematically still treats all signals of the circuit to be at the same frequency ω, so that the resultant analysis related to reciprocity becomes compatible with prior network theories. The key enabler to such a treatment is to model the additional frequency shifts (i.e., ω_{M} in Fig. 3) as explicit changes of the *time & space-varying phases* in the complex amplitudes (i.e., $V_{1,2}^{\pm}$ in Fig. 6) of the time-harmonic waves. Correspondingly, the two-port BFC, now treated as a processor to waves at ω, is described by a 2 × 2, *time/phase-varying* S-parameters matrix at ω (see Fig. 6)

$$\begin{bmatrix} V_1^-(x,t) \\ V_2^-(x,t) \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} V_1^+(x,t) \\ V_2^+(x,t) \end{bmatrix}. \quad (2)$$

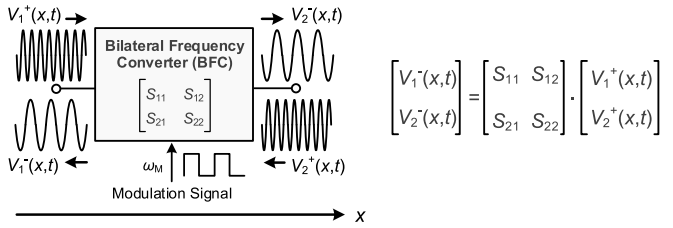


Fig. 6. Modeling the BFC with time/space-varying complex amplitudes and S-parameters at a unified reference frequency of ω.

For the simplicity of our analysis, we examine a down-conversion BFC at $x = 0$ with perfect port matching (hence, $S_{11} = S_{22} = 0$) and zero insertion loss. We also ignore the higher-order harmonic mixing terms. To derive S_{21}, we first investigate the case of a forward signal flow (hence, $V_2^+ = 0$) at an invariant phase velocity of v_p in Fig. 6. The input wave at ω on the left side of BFC is expressed as

$$\mathrm{Input}_{\rightarrow}(x,t) = V_1^+(x,t)e^{j(\omega t - kx)} \tag{3}$$

where $k = \omega/v_\mathrm{p}$ is the wave propagation constant at ω. Note that the $V_1^+(x,t)$ in this case is not time/space-dependent, because the total phase variation at varying t and x is already explicitly given in the $e^{j(\omega t-kx)}$ term. Next, we assume the mixer is driven by a modulation signal with the frequency of ω_M and the phase of φ_M. Accordingly, the output wave on the right side of the mixer, generally expressed as

$$\mathrm{Output}_{\rightarrow}(x,t) = V_2^-(x,t)e^{j(\omega t - kx)} \tag{4}$$

is a frequency down-shifted version of the input wave, hence, can also be expressed as

$$\mathrm{Output}_{\rightarrow}(x,t) = V_1^+ e^{j[(\omega-\omega_\mathrm{M})t-(k-k_\mathrm{M})x+\varphi_1]} \tag{5}$$

where $k_\mathrm{M} = \omega_M/v_\mathrm{p}$ represents the change of wave propagation constant due to the frequency shifting. To determine the phase φ_1 in (5), we note that, at the BFC position ($x = 0$), the initial ($t = 0$) phase difference between the input and output waves is the phase of the modulation signal, therefore

$$\varphi_1 = -\varphi_\mathrm{M} \tag{6}$$

and

$$\begin{aligned}\mathrm{Output}_{\rightarrow}(x,t) &= V_1^+ e^{j[(\omega-\omega_\mathrm{M})t-(k-k_\mathrm{M})x-\varphi_\mathrm{M}]}\\ &= V_1^+ e^{j(\omega t-kx)}e^{-j(\omega_\mathrm{M}t-k_\mathrm{M}x+\varphi_\mathrm{M})}.\end{aligned} \tag{7}$$

Comparing (4) and (7), we conclude that

$$V_2^-(x,t) = V_1^+ e^{-j(\omega_\mathrm{M}t-k_\mathrm{M}x+\varphi_\mathrm{M})} \tag{8}$$

which leads to

$$S_{21} = e^{-j(\omega_\mathrm{M}t-k_\mathrm{M}x+\varphi_\mathrm{M})}. \tag{9}$$

Next, for the case of a reverse signal flow (hence, $V_1^+ = 0$), the input and output waves at the right and left sides of BFC, respectively, are expressed as

$$\mathrm{Input}_{\leftarrow}(x,t) = V_2^+ e^{j(\omega t+kx)} \tag{10}$$

$$\mathrm{Output}_{\leftarrow}(x,t) = V_1^-(x,t)e^{j(\omega t+kx)}. \tag{11}$$

Similar to the previous case, the actual input frequency is ω, and hence, V_2^+ here is not time/space-dependent. And the output wave is, again, a frequency down-shifted version of the input, and can be derived as

$$\mathrm{Output}_{\leftarrow}(x,t) = V_2^+ e^{j[(\omega-\omega_\mathrm{M})t+(k-\omega_M)x-\varphi_\mathrm{M}]} \tag{12}$$

$$= V_2^+ e^{j(\omega t+kx)}e^{-j(\omega_\mathrm{M}t+k_\mathrm{M}x+\varphi_\mathrm{M})} \tag{13}$$

which leads to

$$V_1^-(x,t) = V_2^+ e^{-j(\omega_\mathrm{M}t+k_\mathrm{M}x+\varphi_\mathrm{M})} \tag{14}$$

and

$$S_{12} = e^{-j(\omega_\mathrm{M}t+k_\mathrm{M}x+\varphi_\mathrm{M})}. \tag{15}$$

In summary, the S-parameters matrix for an ideal BFC is asymmetric ($[S] \neq [S]^\mathrm{T}$)

$$\begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} 0 & e^{-j(\omega_\mathrm{M}t+k_\mathrm{M}x+\varphi_\mathrm{M})} \\ e^{-j(\omega_\mathrm{M}t-k_\mathrm{M}x+\varphi_\mathrm{M})} & 0 \end{bmatrix} \tag{16}$$

which indicates that the BFC is a non-reciprocal component.[3] That also explains why the combination of a BFC and reciprocal filters enables non-reciprocal signal flows in Fig. 3. Lastly, we also notice that in [17], a criterion is suggested to judge whether a structure has non-reciprocity: the structure should function as an isolator that can suppress a back-reflected wave with the same mode and frequency as the forward output wave. In Fig. 4, if we assume the input (at ω_TX) is at the TX port, the output (at ω_ANT) is at the ANT port, and the RX port is terminated with a matched load (so that the circuit is a two-port structure), it is easy to see that a back-reflected wave (at ω_ANT) at the output ANT port does not transmit back to the input TX port. The above criterion is therefore, met.

C. Discussions

As described in Section I, isolation in prior magnetic-free circulators is prone to any incomplete out-of-phase cancellation of the TX signal within two different paths. Here, we examine the robustness of isolation in our scheme. We first note that similar incomplete signal cancellation also happens with the inevitable presence of 1) different signal loss within the four paths, due to the mismatches of switch transistors and phase shifters, and 2) non-ideal duty cycle and quadrature phases of the modulation clock. Fortunately, as Fig. 5(a) indicates, the existence of the above problems only results in the un-canceled TX-to-ANT signal residuals at $\omega_\mathrm{ANT}+\omega_\mathrm{M}$ and $\omega_\mathrm{ANT}+2\omega_\mathrm{M}$, which is far away from ω_ANT and can be easily filtered. Similarly, for the ANT to RX direction [Fig. 5(b)], the residuals are located at $\omega_\mathrm{RX}+\omega_\mathrm{M}$ and $\omega_\mathrm{RX}+2\omega_\mathrm{M}$, which can also be readily filtered out. We also note that such robust isolation applies to a broad operation band: although the phase $\Delta\varphi$ applied by each shifter only remains precise within a narrowband, the imperfect vector cancellation in Fig. 5 at large frequency offset does not lead to TX-to-RX leakage.

[3] Although the location of the BFC is assumed to be at $x = 0$, this condition, however, should not be applied to (16), because the $e^{jk_\mathrm{M}x}$ terms describe how the extra space-dependent phases of the output waves in opposite directions are affected by the BFC: one decreases with x, while the other one increases with x. Such non-reciprocity is introduced by the frequency shift (hence, non-zero k_M), or more essentially, the time-variant nature of the BFC.

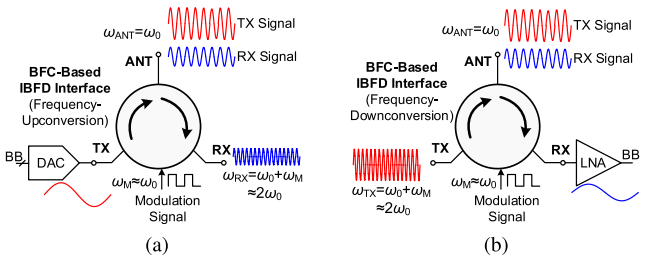


Fig. 7. BFC-based IBFD circuits that provide direct baseband-RF conversion for (a) transmitter path and (b) receiver path.

The presented circuit has a few more advantages in addition to the improved isolation and bandwidth. Cryogenic quantum platforms are highly sensitive to heat generation. Fewer transistor switches of our scheme lead to lower total clock signal dissipation at the gates of the transistors,[4] which sets the intrinsic power consumption (i.e., generated heat) of the IBFD circuit. In addition, by choosing ω_M to be close to ω_0, the circuit can also perform the additional function of receiver down-mixing; as a result, a dedicated down-conversion mixer succeeding the RX port is no longer needed. Basically, it is a mixer-first receiver that typically has higher linearity and blocker tolerance, but degraded sensitivity compared with standard receivers. As illustrated in Fig. 7(a), the BFC can also be designed to perform frequency up-conversion, which can turn it into a direct digital-to-RF transmitter. It is noteworthy that the basic scheme in Fig. 3 does not provide quadrature frequency mixing needed for quadrature amplitude modulation (QAM). One more path consisting of an additional duplexer and switch bank can be added to implement the I/Q paths. Such a quadrature IBFD interface would still be compact because the modulation clock generator and the quadrature Lange coupler can be shared between the two paths.

The large ω_M value in Fig. 7, which may increase ω_{TX} or ω_{RX} to up to $2\omega_0$, can degrade the transmitter power efficiency or the receiver noise figure (NF) and gain. Fortunately, the f_T/f_{max} in deep-submicrometer CMOS technology nodes are much higher than our targeted gigahertz-level operation frequency, so the above performance compromise is small. A smaller ω_M can always be chosen to further reduce the above compromise, but that comes with the expense that a higher filter order in the duplexer is required. Although a direct TX-to-RX leakage through the filters is at a different frequency from ω_{RX}, it should still be sufficiently suppressed, so as not to desensitize the low-noise amplifier connecting to the RX port. Suppose we set ω_M to be $\omega_0/2$ in Fig. 4 (i.e., $\omega_{TX} = 3\omega_0/2$, $\omega_{RX} = \omega_0/2$), a three-pole LPF (with -60 dB/dec roll-off) can already provide a TX-to-RX isolation of $\sim$30 dB. High-order filters, of course, inevitably increase the die size and filter loss in a fully-integrated system. In sum, the best design strategy should be determined by the specific operation frequency,

[4]Note that it is different from the well-known dynamic power ($CV_{DD}^2 f_{CLK}$) of digital circuits because the heat associated with that dynamic power is not generated within the switches (but in the clock generator which can be placed outside of the cryogenic environment). Instead, the dissipation referred here relates to the ac power loss of the clock signal in the switch transistors due to their gate and channel resistance.

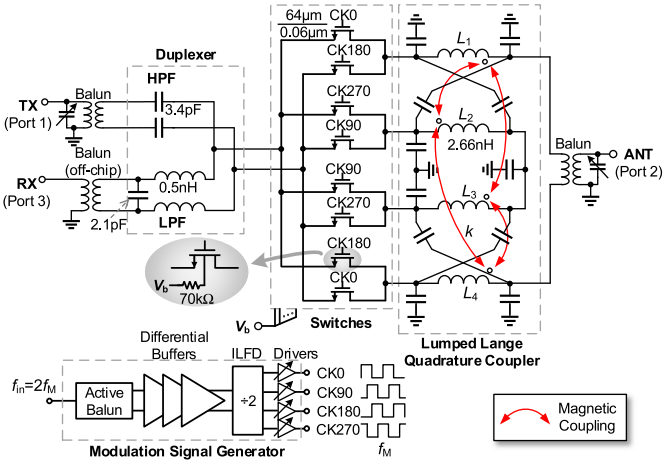


Fig. 8. Schematic of the 4-GHz BFC-based IBFD interface.

CMOS process, as well as the specifications of other TX and RX blocks.

III. Circuit Implementations of a 4-GHz IBFD Interface

To experimentally demonstrate the presented scheme, a CMOS BFC-based IBFD interface with 4-GHz ANT frequency is prototyped. Its design details and simulation results are provided in this section.

A. BFC-Based IBFD Interface

The full schematic of the BFC-based IBFD interface is shown in Fig. 8. One goal of this design is to showcase an integrated down-mixing function; correspondingly, f_M is chosen to be $f_{ANT} = 4$ GHz, and hence, f_{TX} is $f_{ANT} + f_M = 8$ GHz. To suppress undesired signal/clock feedthrough in the switches at f_{TX}, f_{ANT}, and f_M, differential signaling is adopted in the circuit. Each differential switch pair in Fig. 8 has a transistor size of 64 μm/0.06 μm. A pair of 3.4-pF MIM capacitors are used as the HPF at the TX port, and an *L*-*C* LPF is employed at the RX port. To facilitate the single-ended testing of the chip, two on-chip baluns are implemented at the TX and ANT ports, and one off-chip balun is used at the RX port. Each on-chip balun is in shunt with a MOS varactor, in order to provide impedance tuning at the TX and ANT ports. For testing purposes, the chip also has a broadband integrated modulation clock generator to provide the quadrature signals to drive the eight switches.

A differential lumped Lange quadrature coupler is adopted to realize the quadrature-phase-shifting functions at f_{ANT}. Fig. 9 shows the layout of the coupler, which has an equivalent circuit given in Fig. 8. The design is similar to that in [18] but has a differential structure. By adopting both inductive and capacitive coupling, a highly compact size of 0.073 mm^2 is achieved. Shown in Fig. 9(a), the Lange coupler consists of four coupled inductors and metal–oxide–metal (MOM) capacitors (placed under the inductors). The inductors are laid out symmetrically and each one has about 2.5 turns, so that the four quadrature ports are at one side of the coupler and the differential ports are at the other side. Fig. 9(b)–(d) presents

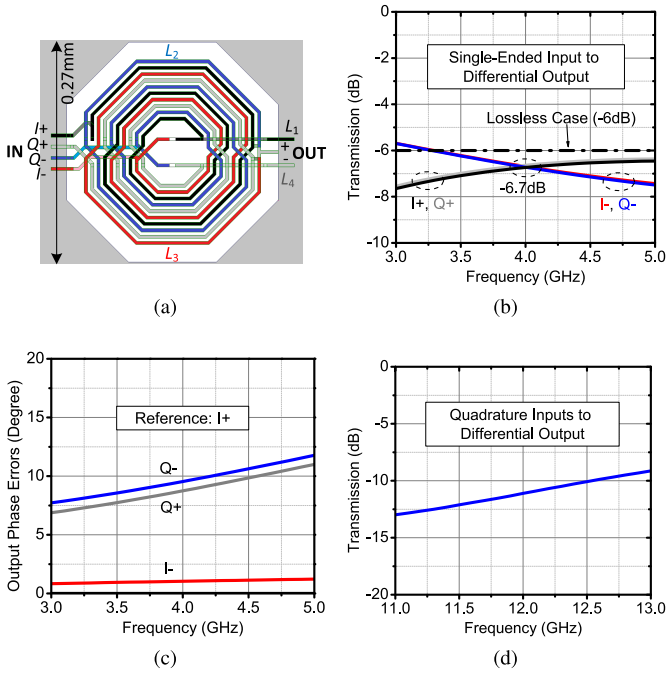


Fig. 9. 4-GHz quadrature Lange coupler: (a) geometry, (b) and (c) simulated transmission amplitude and phase at f_{ANT}, and (d) simulated transmission of the upper-sideband frequency component at $f_{\mathrm{TX}} + f_{\mathrm{M}}$.

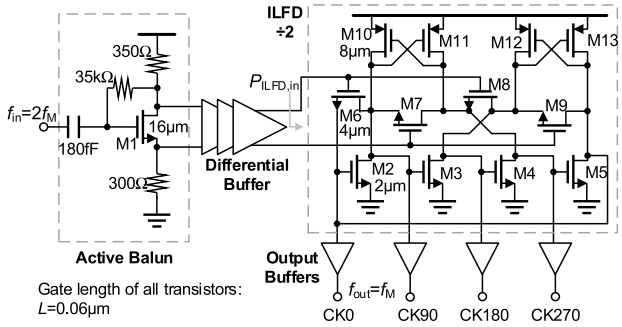


Fig. 10. Schematic of the 4-GHz modulation clock generator.

the HFSS-simulated results of the quadrature coupler. The simulated conversion loss at 4 GHz is about 0.7 dB, and the simulated return loss is less than −10 dB for all ports.

In Fig. 5(a), the frequency component at $\omega_{\mathrm{TX}} + \omega_{\mathrm{M}}$ (∼12 GHz) is canceled upon the application of the phases in the shifters. In our circuit prototype, such an operation is instead realized by the bandpass characteristic of the quadrature coupler: shown in Fig. 9(d), the transmission at 12 GHz is directly blocked by the coupler.

The modulation clock generator consists of one active balun, a three-stage differential buffer, an injection-locked frequency divider (ILFD), and output drivers as shown in Fig. 10. A self-biasing common-source/drain amplifier is used as a broadband active balun. The subsequent three-stage differential buffer then provides additional common-mode suppression. The divide-by-2 ILFD consists of two pMOS latches (M10–M13), an nMOS ring oscillator (M2–M5), and an nMOS injection network (M6–M9). The pMOS latches provide a negative resistance for the ring oscillator. The injection network has four end-to-end connected transistors

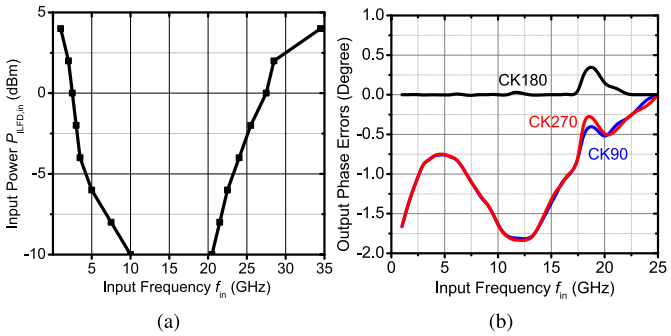


Fig. 11. Simulated (a) locking-range of ILFD and (b) output phase errors of the modulation clock generator.

forming a ring. The symmetric topology of the circuit enables an ultra-wide operation range; as shown in Fig. 11(a), the simulated input locking-range of ILFD can be as wide as 1–35 GHz, when the injected power is 4 dBm. The modulation clock generator is, therefore, capable of providing an output at 0.5–12.5 GHz, which is limited by the phase imbalance of active balun. Lastly, as Fig. 11(b) shows, the phase errors of the output across the wide operation frequency are below 2°, which is again mainly due to the symmetry of the circuit topology. The simulated dc power of the block is 42 mW. It is worth noting that this modulation clock generator is over-engineered, in light of the large operation temperature range and the unavailability of the device models under cryogenic conditions. In the future, more efficient (and narrowband) sources based on *L*-*C* oscillators could be adopted, which should reduce the power to a few milliwatt [19]. The simulated power dissipation of the IBFD core, which is essentially the net clock signal power injection into the eight switching transistors due to their gate and channel resistance, is 0.4 mW at $f_{\mathrm{M}} = 4$ GHz. That sets the ultimate cooling budget of the circuit used in a cryogenic system if we assume that the clock generator is outside of the cryostat, or shared among many IBFD cores.

As discussed in Section II, our circuit is robust against the process-voltage-temperature (PVT) variations.[5] To verify that the simulated TX-to-RX isolation of the IBFD core circuit with 50-Ω matching at the ANT port is shown in Fig. 12. With no variation, the TX-to-RX isolation is better than 42 dB across the whole operation frequency. Fig. 12 also shows that, even with a 20° modulation clock mismatch among different paths, the isolation is still better than 30 dB. In another extreme case, where the size of half of the switches is increased by 100%, the simulation shows that the isolation is better than 34 dB. With a 10% mismatch of quadrature Lange coupler, the isolation is better than 33 dB. The variation of the duplexer also has a negligible impact on the isolation, due to the large TX and RX frequency difference. All these are a strong indication about the robustness of the isolation. Lastly,

[5]Since in our design $\omega_{\mathrm{M}} = \omega_{\mathrm{ANT}}$, one potential isolation concern is that the residual at $\omega_{\mathrm{TX}}+\omega_{\mathrm{M}}$ in Fig. 5(a) would be leaked to the RX port through 1) the reflection by the ANT and then 2) a high-order mixing with the $3\omega_{\mathrm{M}}$ signal in the ANT-to-RX direction. Fortunately, a phasor-diagram analysis similar to that in Fig. 5 reveals that the above third-order down-converted components inside the four BFC paths cancel each other. Hence, the TX-to-RX leakage via the stated mechanism is insignificant.

TABLE I
COMPARISON WITH STATE-OF-THE-ART INTEGRATED CIRCULATORS IN CMOS

	This Work		[11]		[5]	[6]	[7]	[8]
	300K	4.2K	300K	4.2K				
Frequency (GHz)	3.4∼4.6		5.6∼7.4	5.8∼7.6	0.65∼0.85	0.86∼1.08	22.7∼27.3	50∼56.8
Fractional Bandwidth	30%		28%	26.9%	26.7%	17%	18%	14.6%
Minimum Isolation (dB)	32	14	18	17	15	25	18.5	20
Minimum TX-to-ANT Loss (dB)	3.0	1.9	2.2	1.3	1.7	2.1	3.3	3.6
Minimum ANT-to-RX Loss (dB)	3.2	2.0	2.2	1.3	1.7	2.9	3.2	3.1
Noise Figure (dB)	5.8/5.9[(a)]	N/A	2.4	N/A	4.3	3.1	3.3	3.2
TX-to-ANT / ANT-to-RX IIP3 (dBm)	29.5/27.6	N/A	>18.7	>18.1	27.5/8.7	50.0/36.9	20.1/19.9	19.4/19.0
TX-to-ANT / ANT-to-RX IP1dB (dBm)	11.4/11.1	11.0/11.0	N/A	N/A	N/A	>30.7/ 21.0	>21.5/ >21.0	>19.7/ >19.1
Elimination of On-Chip TX-to-RX Coupling ?	Yes		No		No	No	No	No
RX Down-Mixing ?	Yes		No		Yes	No	No	No
Fully Integrated ?	Yes		Yes		No	Yes	Yes	Yes
DC Power [(b)] (mW)	48	42.6	12.4	10.5	59	170	78.4	41
Core Area (mm^2) (Wavelength Scale)	0.27 (λ^2/20778)		0.45 (λ^2/4727)		25 (λ^2/6390)	16.5 (λ^2/5500)	2.16 (λ^2/67)	1.72 (λ^2/18)
CMOS Technology	65-nm Bulk		40-nm Bulk		65-nm Bulk	180-nm SOI	45-nm SOI	45-nm SOI

[(a)] SSB mixer NF reported here. With TX off/on (0 dBm) and the homodyne RX down-conversion function included.
[(b)] Mainly from the modulation clock generator. The simulated power dissipation of our IBFD core circuit is ∼0.4 mW.

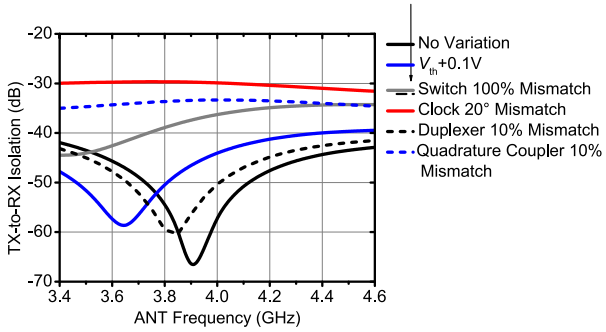


Fig. 12. Simulated TX-to-RX isolation of the 4-GHz IBFD interface.

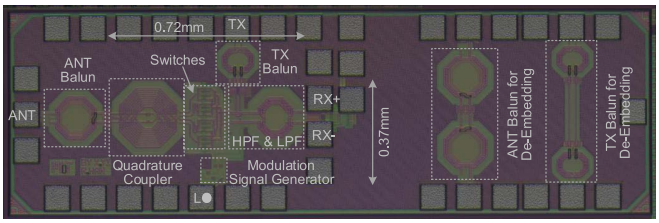


Fig. 13. Die photographs of 4-GHz BFC-based IBFD interface, and the back-to-back balun structures for deembedding.

to evaluate the impact of possible device behavior changes under cryogenic conditions (e.g., threshold voltage V_{th} increase as reported in [20]), we increase the V_{th} of transistors by 0.1 V, and observe that the minimum isolation degrades by only 3.7 dB. We are currently unable to estimate the impact of the increased substrate resistivity that is due to the freeze-out at cryogenic condition, but we anticipate that the effect should improve the insertion loss of the circuit due to smaller signal leakage from the source/drain to the substrate.

IV. MEASUREMENT RESULTS

The BFC-based full-duplex chip is fabricated using Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm bulk CMOS technology. The die photo is shown in Fig. 13. The core IBFD circuit including the quadrature coupler, switches, modulation signal generator, HPF, and LPF occupies an area of only 0.27 mm^2. When used in a complete wireless system, the baluns at three ports are not needed, because the ANT and the TX/RX circuitry are normally differential. So, to test the performance of the core circuit of the chip, standalone structures consisting of back-to-back ANT, and TX baluns are also fabricated for de-embedding purpose. The low-frequency off-chip balun at the RX port is also measured and de-embedded through a back-to-back structure on a printed circuit board (PCB). The chip is characterized at both room temperature (∼300 K) and cryogenic temperature (∼4.2 K). Fig. 14(a) shows the setup for ANT-to-RX measurement at room temperature. In this setup, the RF performance is tested through the probing on the high-frequency pads [ANT, TX, and local oscillator (LO)]. The low-frequency RX differential ports are wire-bonded to the PCB and connected to an off-chip balun. Power supplies and bias voltages are also wire-bonded and supplied externally.

A Keysight performance network analyzer (PNA)-X network analyzer (N5245B) with a mixer-measurement configuration is utilized, and it is calibrated with −30 dBm stimulated power. The LO port of the PNA delivers the ∼8-GHz ($2f_M$) modulation. To test the TX-to-ANT transmission, the other two ports of the PNA (Port 1 and 2) for cross-frequency S-parameter measurement are connected to the TX and ANT ports, respectively, and the RX port is terminated with 50 Ω. The measured ANT frequency is from 3.4 to 4.6 GHz. Shown in Fig. 15(a) are the measured S-parameters after de-embedding the loss of the baluns. The TX-to-ANT insertion loss extracted from S_{21} ranges from 3.0 to 5.8 dB across the 30% fractional bandwidth. As expected, S_{12} that represents

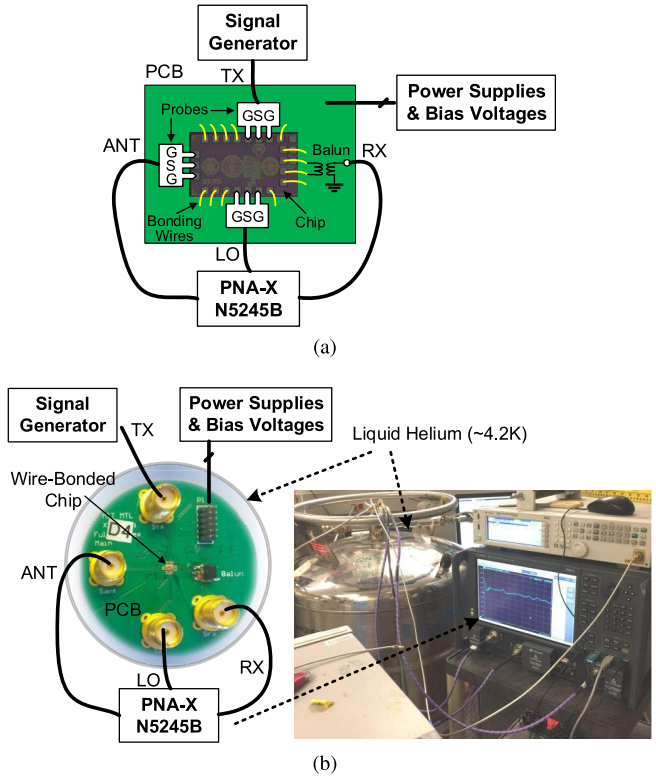


Fig. 14. Setups for the ANT-to-RX measurement at (a) room temperature (around 300 K) and (b) cryogenic temperature (around 4.2 K). The modulation signal is injected through the LO port.

the reverse insertion from ANT to TX is below −10 dB, hence, the non-reciprocity. Next, the two PNA ports (dubbed as Port 2 and Port 3) are connected to the ANT and RX ports, respectively, and the TX port is terminated with 50 Ω. The measured S-parameters are shown in Fig. 15(b). The ANT-to-RX insertion loss extracted from S_{32} ranges from 3.2 to 6.1 dB. The measured ANT-to-RX insertion loss does not change when a 0-dBm TX input power is on. Similar to the above case, the reverse RX-to-ANT transmission (S_{23}) is below −10 dB. Lastly, the TX-to-RX isolation is tested by connecting the two PNA cross-frequency ports with the TX and RX ports, respectively, while loading the probed ANT port with 50 Ω. As shown in Fig. 15(c), across the 30% fractional bandwidth, the measured isolation ranges from 25.5 to 43 dB. Note that the balun loss which contributes to additional isolation has already been de-embedded. Similar to all other full-duplex systems, the wave reflection at the ANT port degrades the isolation performance. With an impedance tuner (Maury Microwave 8045p) at the ANT port, the measured isolation improves to 32–50 dB.

The setup shown in Fig. 14(a) is also used to test the NF performance of the chip. To emulate the full-duplex operation, an extra signal generator is also connected to the TX port to provide a simultaneously transmitted TX power of 0 dBm. With the TX power turned off, the measured NF shown in Fig. 15(d) has a minimum value of 5.8 dB. With the TX power turned on, unlike the significant NF degradation in full-duplex mode in [5], we observe only <1 dB NF degradation at some baseband frequencies. That again illustrates excellent isolation between the TX and RX

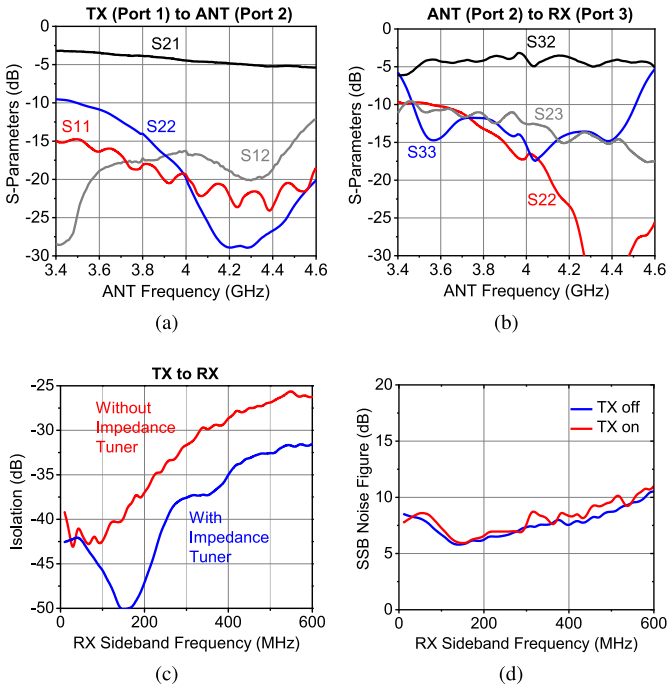


Fig. 15. Measured results of BFC-based IBFD interface at 300 K: (a) TX-to-ANT, (b) ANT-to-RX, (c) TX-to-RX paths S-parameters, and (d) SSB NF of the ANT-to-RX path.

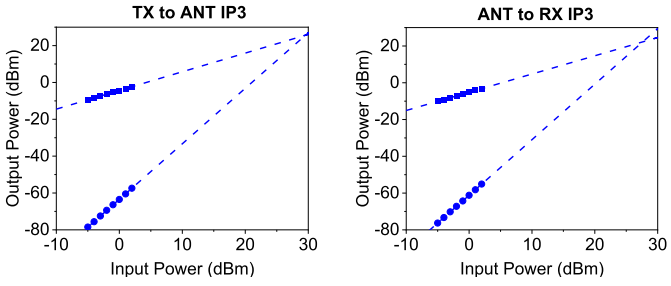


Fig. 16. Measured IP3 of BFC-based IBFD interface at 300 K: (a) TX-to-ANT and (b) ANT-to-RX paths.

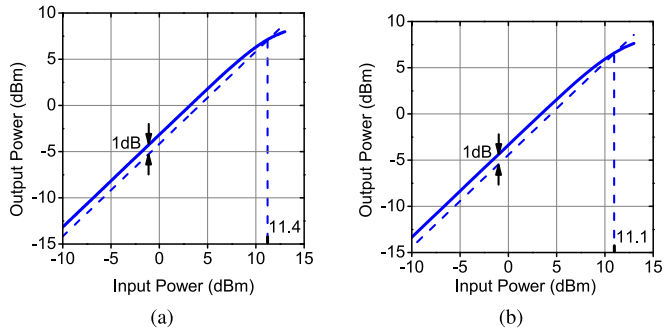


Fig. 17. Measured P1dB of (a) TX-to-ANT and (b) ANT-to-RX at 300 K.

paths. It is important to note that, since the presented circuit performs the homodyne down-conversion, the noise at both the upperside and lower side bands around f_{ANT} is folded to the RX baseband output. Therefore, the data shown in Fig. 15(d) are in fact the SSB NF, which assumes that the input signal only lies at one sideband around f_{ANT}. That explains why the NF in Fig. 15(d) is on average ∼3 dB larger than the

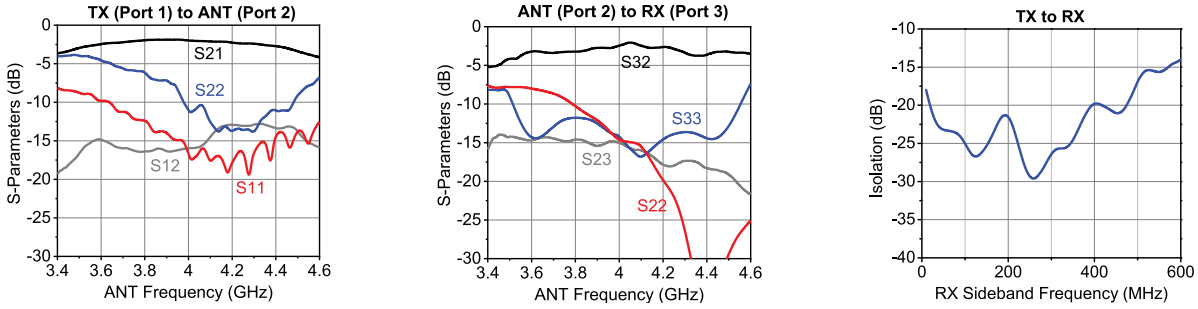


Fig. 18. Measured results of BFC-based IBFD interface at 4.2 K: cross-frequency S-parameters for (a) TX-to-ANT, (b) ANT-to-RX, and (c) TX-to-RX paths.

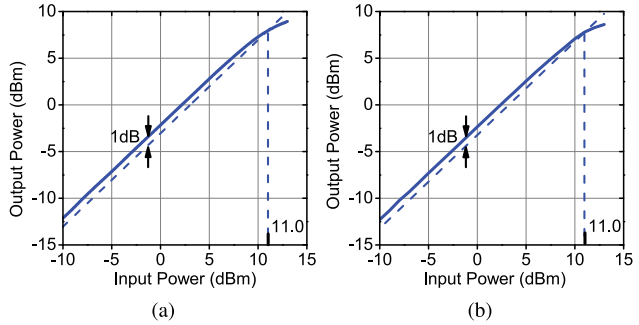


Fig. 19. Measured P1dB of (a) TX-to-ANT and (b) ANT-to-RX at 4.2 K.

insertion loss in Fig. 15(b). With additional filtering of the noise from one sideband, it is possible that the NF could be improved in future developments. Also note that due to the integrated receiver down-conversion function of our scheme, further baseband amplification beyond our IBFD interface would incur less additional noise/power penalty, compared to the RF amplification in traditional IBFD systems.

The linearity of the circuit is also measured by sweeping the input power of the setup. To improve the linearity, the power supply of the LO circuit is increased to 1.4 V. In addition, the body bias voltage of the deep N-well switches is set to −0.5 V to reduce the effects of the parasitic pn junctions between S/D and the body, and enhance the linearity and the power handling of switches [21]. The measured results are given in Fig. 16, where the IIP3 for the TX-to-ANT and ANT-to-RX directions are 29.5 and 27.6 dBm, respectively. The measured input P1dB (IP1dB) of TX-to-ANT and ANT-to-RX at 300 K are 11.4 and 11.1 dBm, respectively, as shown in Fig. 17.

To test the IBFD interface performance under cryogenic conditions, a setup shown in Fig. 14(b) is used, where a PCB with the wire-bonded chip is placed inside liquid helium (4.2 K) and is connected to the same Keysight PNA-X through cables. The wire-bonded ANT and TX baluns, as well as the off-chip balun are de-embedded through *ABCD*-parameters. The measured results are shown in Fig. 18. Compared to the TX-to-ANT transmission at 300 K, the one at 4.2 K is improved to 1.9–4.2 dB [Fig. 18(a)], which is probably due to the higher carrier mobility, higher substrate resistivity (hence, lower leakage to the substrate), and lower metal resistivity (hence, higher quality factor of passive components) [22], [23]. Similarly, the measured ANT-to-RX insertion loss is also improved to 2.0–5.3 dB at 4.2 K. Since the ANT port is connected through a bond wire in Fig. 14(b), rather than through probing in the 300-K case, the bond wire inductance causes an impedance mismatch that cannot be fully compensated by the impedance tuner through the cable. The associated wave reflection at the ANT port, therefore, degrades the TX-to-RX isolation. As shown in Fig. 18(c), the measured isolation ranges from 14 to 29.5 dB across the whole operation band. The measured IP1dB of TX-to-ANT and ANT-to-RX are both 11.0 dBm at 4.2 K, as shown in Fig. 19. In the measurements at both 4.2 and 300 K, the LO leakage power at the ANT port is about −42 dBm.

The NF measurement under cryogenic conditions requires the insertion of a calibrated attenuator and a low-noise amplifier (both placed inside liquid helium) into the ANT and RX ports of the circuit, respectively. The former is to suppress the high 300-K noise from the PNA-X and to create a 4.2-K noise reference; and the latter is to amplify the circuit output noise to ensure accurate measurement by the PNA-X. Due to the instrument limitation, we are not able to perform such testing. Theoretically, the thermal noise of the active and passive devices scale down with the temperature, so similar to the 300-K case, the NF value (with reference to 4.2 K) is expected to be still dominated by both the ANT-RX insertion loss (∼2 dB at 4.2 K) and the noise folding effect (∼3 dB). The noise temperature of the circuit is, therefore, estimated to be ∼9 K. Similar to that in [11], our estimation also does not include the impact of phase noise in the clock.

The measured power consumption of the chip, which is almost entirely from the integrated modulation clock generator, is 48 mW at 300 K and 42.6 mW at 4.2 K.

V. Conclusion

A new concept using frequency conversions of two counter-propagating signals is demonstrated, which performs non-reciprocity similar to that in circulators and enables IBFD systems in CMOS. In this article, a 4-GHz IBFD front-end interface is implemented to demonstrate this scheme. Its performance is summarized in Table I, along with a comparison with other state-of-the-art integrated circulators in CMOS. One notable advantage of our front-end is the high TX-to-RX isolation across a wide operation frequency thanks to the widely separated TX and RX frequencies and the robustness

against path mismatch and non-ideal clocking. As described in Section III, the integrated broadband quadrature modulation clock generator is over-engineered, leading to higher dc power compared to some works in the table; the problem should be alleviated with a more optimized narrowband clock generator design or with a more advanced CMOS technology node. Similar to the situation of other CMOS circulator works, the heat dissipation of the passive IBFD core the circuit is low (∼0.4 mW in simulation), so the presented scheme may be applicable for quantum platforms when the clock generation is outside of the cryogenic fridge and/or is shared among multiple IBFD units. It is also worth mentioning that, due to the simple construction of the presented scheme, a highly compact circuit area, when normalized to the square of wavelength, is achieved (see Table I).

ACKNOWLEDGMENT

The authors would like to thank Kathleen Howard and Richard Hoft at Keysight for their generous support of testing equipment, and Prof. Karl K. Berggren at MIT for his support in the cryogenic circuit testing and feedback to the article. The authors also thank Prof. Harish Krishnaswamy at Columbia University for the technical discussions. Any opinions, findings, conclusions, or recommendations expressed in this material are those of the authors and do not necessarily reflect the views of the United States Air Force. This is the extended version of an article originally presented at the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, Los Angeles, CA, USA, August 2020.

REFERENCES

[1] K. E. Kolodziej, B. T. Perry, and J. S. Herd, "In-band full-duplex technology: Techniques and systems survey," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 3025–3041, Jul. 2019.

[2] N. Reiskarimian, A. Nagulu, T. Dinc, and H. Krishnaswamy, "Nonreciprocal electronic devices: A hypothesis turned into reality," *IEEE Microw. Mag.*, vol. 20, no. 4, pp. 94–111, Apr. 2019.

[3] L. Ranzani and J. Aumentado, "Circulators at the quantum limit: Recent realizations of quantum-limited superconducting circulators and related approaches," *IEEE Microw. Mag.*, vol. 20, no. 4, pp. 112–122, Apr. 2019.

[4] N. Reiskarimian and H. Krishnaswamy, "Magnetic-free non-reciprocity based on staggered commutation," *Nature Commun.*, vol. 7, no. 1, pp. 1–10, Sep. 2016.

[5] N. Reiskarimian, J. Zhou, and H. Krishnaswamy, "A CMOS passive LPTV nonmagnetic circulator and its application in a full-duplex receiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1358–1372, May 2017.

[6] A. Nagulu, A. Alu, and H. Krishnaswamy, "Fully-integrated non-magnetic 180nm SOI circulator with > 1W P1dB, >+50dBm IIP3 and high isolation across 1.85 VSWR," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2018, pp. 104–107.

[7] T. Dinc, A. Nagulu, and H. Krishnaswamy, "A millimeter-wave non-magnetic passive SOI CMOS circulator based on spatio-temporal conductivity modulation," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3276–3292, Dec. 2017.

[8] A. Nagulu and H. Krishnaswamy, "28.5 non-magnetic 60GHz SOI CMOS circulator based on loss/dispersion-engineered switched bandpass filters," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 446–448.

[9] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A 6.5-GHz cryogenic all-pass filter circulator in 40-nm CMOS for quantum computing applications," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 107–110.

[10] J. Zhou *et al.*, "Integrated full duplex radios," *IEEE Commun. Mag.*, vol. 55, no. 4, pp. 142–151, Apr. 2017.

[11] A. Ruffino, Y. Peng, F. Sebastiano, M. Babaie, and E. Charbon, "A wide-band low-power cryogenic CMOS circulator for quantum applications," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1224–1238, May 2020.

[12] A. Poon, A. Chang, H. Samavati, and S. S. Wong, "Reduction of inductive crosstalk using quadrupole inductors," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1756–1764, Jun. 2009.

[13] X. Yi, J. Wang, C. Wang, K. E. Kolodziej, and R. Han, "A 3.4–4.6GHz in-band full-duplex front-end in CMOS using a bi-directional frequency converter," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 47–50.

[14] S. Qin, Q. Xu, and Y. E. Wang, "Nonreciprocal components with distributedly modulated capacitors," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 10, pp. 2260–2272, Oct. 2014.

[15] J. R. Carson, "A generalization of the reciprocal theorem," *Bell Syst. Tech. J.*, vol. 3, no. 3, pp. 393–399, Jul. 1924.

[16] D. F. Williams, F. Ndagijimana, K. A. Remley, J. A. Dunsmore, and S. Hubert, "Scattering-parameter models and representations for microwave mixers," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 1, pp. 314–321, Jan. 2005.

[17] S. Fan *et al.*, "Comment on 'nonreciprocal light propagation in a silicon photonic circuit,"' *Science*, vol. 335, no. 6064, p. 38, 2012.

[18] D. Ozis, J. Paramesh, and D. J. Allstot, "Integrated quadrature couplers and their application in image-reject receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1464–1476, May 2009.

[19] M. Raj and A. Emami-Neyestanak, "A wideband injection locking scheme and quadrature phase generation in 65nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 261–264.

[20] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and compact modeling of nanometer CMOS transistors at deep-cryogenic temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018.

[21] Y. Jin and C. Nguyen, "Ultra-compact high-linearity high-power fully integrated DC–20-GHz 0.18-μm CMOS T/R switch," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 1, pp. 30–36, Jan. 2007.

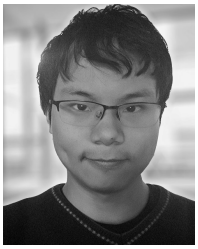
[22] B. Patra *et al.*, "Cryo-CMOS circuits and systems for quantum computing applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 1–13, Jan. 2017.

[23] M. Mehrpoo *et al.*, "Benefits and challenges of designing cryogenic CMOS RF circuits for quantum computers," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2019, pp. 1–5.

Xiang Yi (Senior Member, IEEE) received the B.E. degree from the Huazhong University of Science and Technology (HUST), Wuhan, China, in 2006, the M.S. degree from the South China University of Technology (SCUT), Guangzhou, China, in 2009, and the Ph.D. degree from the Nanyang Technological University (NTU), Singapore, in 2014.

He was a Post-Doctoral Fellow with the Massachusetts Institute of Technology (MIT). He is currently a Professor with SCUT. His research interests include radio frequency (RF), millimeter-wave (mm-wave), and terahertz (THz) frequency synthesizers and transceiver systems.

Dr. Yi was a recipient of the IEEE ISSCC Silkroad Award and SSCS Travel Grant Award in 2013. He is a Technical Reviewer for several IEEE journals and conferences.



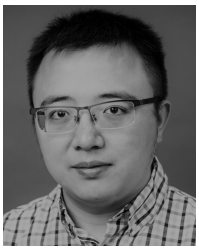
Jinchen Wang (Member, IEEE) received the B.Eng. degree in electronic information engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2019, and the B.Eng. degree (Hons.) in electronics and electrical engineering from the University of Glasgow, Glasgow, U.K., in 2019. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA.

His research interests include RF/mmW/THz circuits, algorithms, and systems for radar imaging, wireless communication, quantum computing, and other novel applications.

Mr. Wang was a recipient of the IEEE Microwave Theory and Technique Society Undergraduate/Pre-Graduate Scholarship Award in 2019.

Marco Colangelo (Graduate Student Member, IEEE) received the B.E. degree in engineering physics and the M.S. degree in nanotechnologies for the ICTS from the Politecnico di Torino, Turin, Italy, in 2015 and 2017, respectively, and the M.S. degree in electronics engineering from the Politecnico di Milano, Milan, Italy, in 2018. He is currently pursuing the Ph.D. degree with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA.

His current research interests include nanofabrication technology, superconducting nanowire microwave devices for information processing and quantum computing systems, and superconducting single-photon detectors for imaging and communication applications.



Cheng Wang (Member, IEEE) received the B.E. degree in engineering physics from Tsinghua University, Beijing, China, in 2008, the M.S. degree in radio physics from the China Academy of Engineering Physics (CAEP), Mianyang, China, in 2011, and the Ph.D. degree from the Department of Electrical Engineering and Computer Science (EECS), Massachusetts Institute of Technology (MIT), Cambridge, MA, USA, in 2020.

He was an Assistant Research Fellow with the Institute of Electronic Engineering, CAEP, Mianyang, China, from 2011 to 2015. Currently, he is a Research Scientist with Analog Devices, Inc. (ADI), Boston, MA, USA. His current research interests include the millimeter/terahertz integrated circuits, and deep learning for wireless communication and automotive radar.

Dr. Wang received the Analog Device, Inc. Outstanding Student Designer Award in 2016, the IEEE Microwave Theory and Techniques Society Boston Chapter Scholarship in 2017, the ISSCC 2018 Student Travel Grant and the 2018 Chinese Government Award for Outstanding Self-Financed Student Abroad, and the MIT Microsystem Technology Laboratory (MTL) 2019 Fall Doctoral Dissertation Seminar Award (one of two students per year in MTL). In 2020, he was granted the IEEE Solid-State Circuit Society (SSCS) Predoctoral Achievement Award.

Kenneth E. Kolodziej (Member, IEEE) received the B.E. and M.E. degrees in electrical engineering from the Stevens Institute of Technology in Hoboken, Hoboken, NJ, USA, in 2007.

In 2017, he joined BAE Systems, Wayne, NJ, to design RF electronics for handheld communication devices. Since 2010, he has been working with MIT Lincoln Laboratory, Lexington, MA, USA, and has conducted research on RF, microwave and photonic circuits, including antenna, radar, and communication systems. He is currently working with the Advanced Technology Division's RF Technology Group, designing compact transceivers and RF cancellation techniques for in-band full-duplex (IBFD) applications. He also teaches an electromagnetics course to undergraduate students at the Massachusetts Institute of Technology (MIT), Cambridge, MA, and several "Build-a-Radar" courses on MIT campus.

Mr. Kolodziej is a member of the IEEE Microwave Theory and Techniques, IEEE Antennas and Propagation, and IEEE Communications Societies, where he reviews papers for several journals and conferences. He also serves on the technical program review committees for the IEEE International Microwave Symposium (IMS), the IEEE International Symposium on Antennas and Propagation (APS), the IEEE International Symposium on Phased Array Systems and Technology (PAST), and the IEEE International Conference on Communications (ICC).

Ruonan Han (Senior Member, IEEE) received the B.Sc. degree in microelectronics from Fudan University, Shanghai, China, in 2007, the M.Sc. degree in electrical engineering from the University of Florida, Gainesville, FL, USA, in 2009, and the Ph.D. degree in electrical and computer engineering from Cornell University, Ithaca, NY, USA, in 2014.

He is currently an Associate Professor with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA, USA. His current research interests include microelectronic circuits and systems operating at millimeter-wave and terahertz frequencies.

He was a recipient of the Cornell ECE Director's Ph.D. Thesis Research Award, the Cornell ECE Innovation Award, the two Best Student Paper Awards of the IEEE Radio-Frequency Integrated Circuits Symposium (2012 and 2017), the IEEE Microwave Theory and Techniques Society (MTT-S) Graduate Fellowship Award, the IEEE Solid-State Circuits Society (SSC-S) Predoctoral Achievement Award. He is the winner of the Intel Outstanding Researcher Award (2019) and the National Science Foundation (NSF) CAREER Award (2017). He has served as an Associate Editor for IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEM (TVLSI) (2019∼), IEEE TRANSACTIONS ON QUANTUM ENGINEERING (2020∼) and a Guest Associate Editor for IEEE TRANSACTIONS ON MICROWAVE THEORY (2019) AND TECHNIQUES, and also serves on the Technical Program Committees (TPC) of IEEE RFIC Symposium, European Microwave Conference, and the 2019 and 2021 Steering Committees of IEEE International Microwave Symposium. He is the IEEE MTT-S Distinguished Lecturer (2020–2022).