19.1 A 110-to-130GHz SiGe BiCMOS Doherty Power Amplifier with Slotline-Based Power-Combining Technique Achieving >22dBm Saturated Output Power and >10% Power Back-Off Efficiency

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The demand for 100+Gbps data-rates in wireless communications has driven the rapid development of silicon-based transceivers in the mm-wave and sub-THz bands. The broad available spectrum in D-band (110 to 170GHz) is attracting interest for short-range and backhaul high-speed communication [1,2]. To overcome the high path loss, a high-power transmitter (TX) or power amplifier (PA) is essential in such systems. However, silicon-based mm-wave PAs encounter several challenges, such as the limited f_T/f_{max} of transistors, low breakdown voltage in CMOS/SiGe transistors, and the considerable loss of passive networks. Additionally, the widely employed high peak-to-average-power-ratio (PAPR) signal poses severe requirements for TXs/PAs, including peak efficiency and power back-off (PBO) efficiency. A solution to these challenges is proposed in this work and resulted in a D-band PA with >22dBm saturated output power (P_{SAT}) and >10% PBO efficiency.

On-chip power-combining techniques, such as stacking multi-finger transistors and passive power combiners, are necessary to increase the mm-wave PA output power (P_{OUT}) in silicon processes. Transformer-based combiners are commonly employed for simultaneous power combining and impedance matching [3]. Unfortunately, existing D-band PAs in silicon exhibit limited P_{OUT} and efficiency, mainly due to increased parasitics, reduced port balance, and lossy output networks [4-6]. Although leveraging current clamping in multiple common-base (CB) stages can enhance the power-added efficiency (PAE), the PAs still cannot offer >10% PBO efficiency [7]. Outphasing and Doherty PAs can improve PBO efficiency at mm-wave frequencies, which are intrinsically narrowband. Supporting wideband signals often needs additional complexity and chip area overhead [8]. Hence, to address the challenges in bandwidth, output power, high peak/back-off efficiency, and area, we propose a compact broadband Doherty-PA prototype with slotline-based power combining, which realizes the following: 1) achieving low-loss 8-way power combining, 2) absorbing the broadband active load modulation into the combiner with a compact area, 3) improving the common-mode rejection via orthogonal electric fields, and 4) efficiently supporting high-order modulation schemes in D-band wireless communication.

A three-λ/4-line-based Doherty output network, including two impedance inverters I and II, can improve the bandwidth by introducing extra resonances (Fig. 19.1.1). To avoid excessive loss and area overhead, it is necessary to replace the impedance inverters with compact structures, such as capacitor loaded λ/4 T-line (TL), lumped element pi-network, and transformer-based network [9]. In the actual device, the output capacitance C_{PA} cannot be ignored. Both the C-L-C and transformer-based networks effectively absorb the C_{PA}. The transformer (TF) can also transform the load impedance to the optimal load impedance and combine the multiway output power. Figure 19.1.1 shows the compact broadband Doherty PA prototype with the 8-way hybrid (parallel-series) power combining, where active load modulation with two impedance inverters is implemented in the power combining network. Parallel power combining is achieved through the capacitive impedance inverter I (an equivalent characteristic impedance $Z_{01}=1/2\pi f_0 C_1$), while series power combining is achieved through the transformer-based impedance inverter II (an equivalent characteristic impedance $Z_{02}=2\pi f_0 N(1-k_m^2)L_P$). In practice, the two negative capacitors ($-C_1$) and the four positive capacitors (C_2) are equivalent to the two physically achievable capacitors. In this work, the parameters are designed to meet the impedance relationship of the symmetrical Doherty PA.

Due to the interwinding capacitance C_M, designing mm-wave PAs with conventional transformer-based power-combining techniques is challenging. C_M allows transmitting the undesired common-mode signal and causes the impedances reflected from the output load back to each port to differ in the combiner. Furthermore, if more than one thick metal layer is not available in the process, the conductor loss of the transformer becomes extremely large. Moreover, the transformer-based layouts have to follow strict pattern density rules to stays within a specific range for each metal layer, which also introduces an additional significant loss. The proposed alternative-magnetic-coupling structure in Fig. 19.1.2, composed of microstrip-to-slotline transitions, is helpful to mitigate the C_M since the electrical fields between the slot and T-line are orthogonal. Figure 19.1.2 also shows the design of the proposed broadband D-band Doherty output network with an 8-way slotline-based power combiner. Although the slotline-based circuits have been analyzed and implemented in some prior designs [10-12], they do not simultaneously exploit the intrinsic active-load-modulation and power-combining capabilities. The merged capacitances of C_2 and $-C_1/2$ are realized by Slot 1, while a custom metal-plate capacitor realizes C_1. Simulations verify that well-balanced ports are achieved for each PA output. The proposed network simultaneously achieves Doherty active load modulation and power combining with a minimum power loss of 1.1dB at 0dB PBO and 1.3dB at 6dB PBO. The 1dB bandwidth is over 105 to 133GHz. The low-loss performance is mainly due to the sub-quarter-wavelength design and the solid metal plate of the slotline consisting of all metal layers and vias. Besides, the proposed slotline-based combiner can easily pass the DRC check without filling with dummy patterns.

Figure 19.1.3 shows the schematic of the proposed PA prototype. The Lange coupler and the modified three-conductor-based power splitter split the input signal with equal power and proper phase to eight Aux./Main paths. Each PA core employs an identical stacked HBT topology to achieve high output power. To increase the power gain, driving amplifiers (DAs) with transformer-based interstage matching are used. Finite common-base (CB) impedance (parallel R_{BB}-C_{BB}) and linearity bias circuits at the PAs and DAs enhance the stability and linearity, respectively. The circuit is implemented in a 0.13μm SiGe BiCMOS process with f_T/f_{max}=350/450GHz. The PA occupies a total 1.11mm^2 chip area and the core area is only 0.58mm^2 (Fig. 19.1.7).

Figure 19.1.4 shows the small-signal S-parameters and large-signal continuous-wave (CW) measurements. The chip is wire-bonded to a PCB and probed for evaluation. The S-parameters are characterized through the Keysight frequency extender N5295AX03 (900Hz to 120GHz) and VDI WR6.5 extenders (110 to 170GHz) connected to the Keysight PNA-X N5247B vector network analyzer. The peak S21 is 21.8dB with a 3dB small-signal bandwidth from 107 to 135GHz. Both input and output are well matched over a wide frequency range. Large-signal CW measurements are performed using a 110-to-170GHz source (VDI WR6.5SGX), D-band driver, and attenuator to provide a variable input power. The power meter (Ceyear 2438PB) is used to perform calibration and measure the output power. At 110/120/130GHz, the PA achieves 22.7/22.6/22.4dBm P_{SAT} with 18.7/17.2/16.1% peak PAE (PAE_{MAX}) and 12.1/11.7/9.8% PAE at 6dB back-off from P_{SAT}. From 104 to 134GHz, the PA consistently achieves >21dBm P_{SAT} with >15% peak collector efficiency (CE_{MAX}). From 110 to 130GHz, the 6dB PBO collector efficiency is over 10%.

Figure 19.1.5 summarizes the modulation test using single-carrier 16-QAM and 64-QAM signals. For an 800MSym/s (4.8Gb/s) single-carrier 64-QAM signal with a 9dB PAPR, the PA achieves 13.81dBm average P_{out} (P_{AVG}) and 8.01% average collect efficiency (CE_{AVG}) with 10.9% EVM at 131GHz. For a 2GSym/s (8Gb/s) single-carrier 16-QAM signal with a 8dB PAPR, the PA achieves 13.74dBm P_{AVG} and 7.88% CE_{AVG} with 11.6% EVM at 131.5GHz. However, the measurement performance is limited by the bandwidth limitations of the Tx/Rx modules used for up/downconverter.

In summary, this D-band Doherty PA with 8-way slotline-based power combiner simultaneously achieves high output power and high peak/back-off efficiency. The PA also demonstrates the highest P_{OUT} and PAE at back-off among D-band silicon PAs in Fig. 19.1.6.

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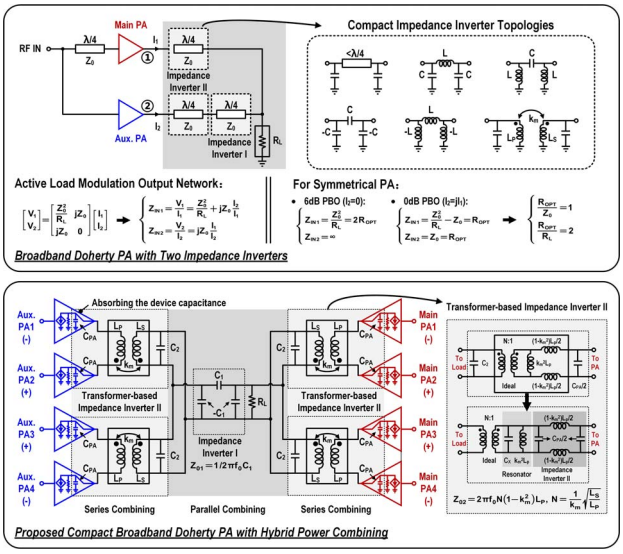

Figure 19.1.1: Conventional broadband Doherty PA with two impedance inverters and the proposed compact broadband Doherty PA with a hybrid power-combining technique.

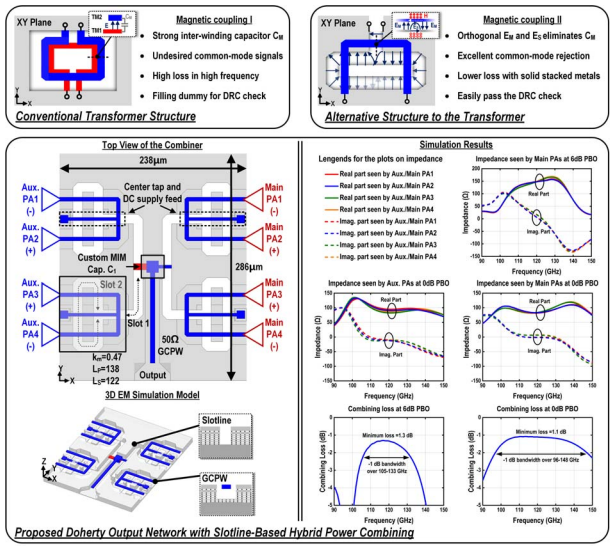

Figure 19.1.2: Implementation of the transformer-based impedance inverter and the simulation results of the proposed compact Doherty output network with slotline-based hybrid power combining.

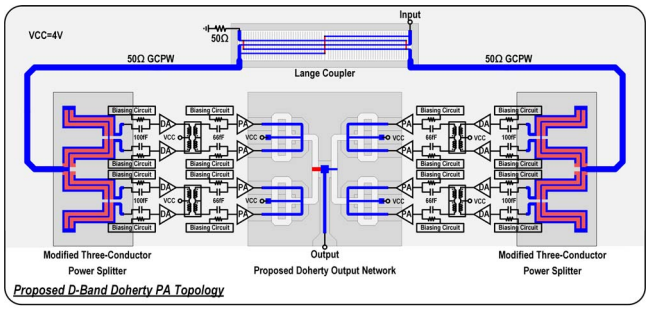

Figure 19.1.3: Schematic of the proposed D-band Doherty PA, a detailed amplifier core, biasing circuit, and the simulation results of the Lange coupler and splitter.

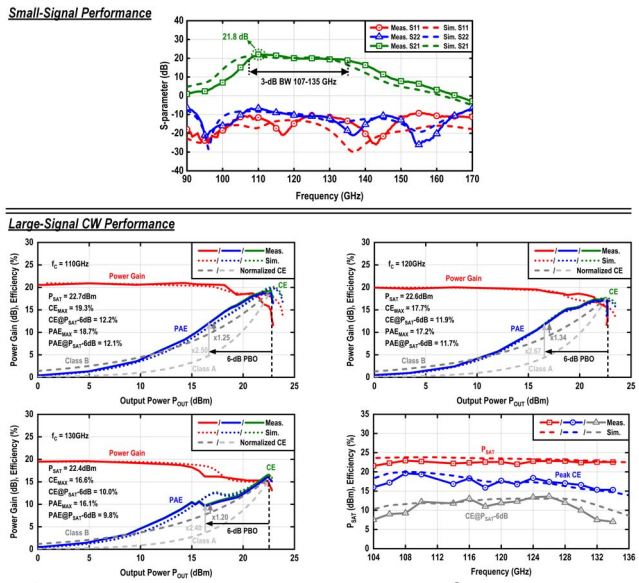

Figure 19.1.4: Measured small-signal and large-signal CW performance of the D-band Doherty PA.

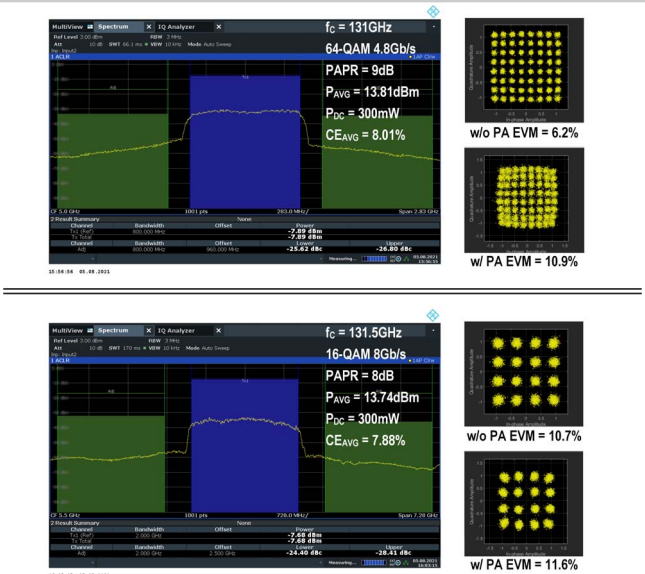

Figure 19.1.5: Modulation measurements of the presented PA using 64-QAM and 16-QAM single-carrier signals, respectively.

Reference	This Work			[4] Philippe ISSCC'20	[5] Li RFIC'21	[7] Petricli MWCL'21		[6] Rao MWCL'21	[8] Liu IMS'21	[3] Kaymaksut T-MTT'15		[2] Hamani SSCL'20	
Technology	130 nm SiGe			16 nm FinFET	45 nm CMOS SOI	55 nm SiGe		90 nm SiGe	130 nm SiGe	40 nm CMOS		45 nm CMOS SOI	
Architecture	8-way Slotline-based Comb. Doherty			4-way TF-based Comb.	8-way TL-based Comb.	Common-base		4-way Wilkioson Comb.	Quadrature Hybrid Doherty	8-way TF-based Comb. Doherty		Tx Front-End (IF AMP+LO+Mixer+PA)	
Supply (V)	4			1	1.2	2.2	2.2	4***	3.6	1.5		1	
Peak Gain (dB)	21.8			25.6	24	24	22.4	18.2	18.5	12	20	22.5****	
BW_{-3dB} (GHz)	28 (107 to 135)			22	21 (130 to 151)	34 (125 to 159)	25 (125 to 150)	35 (110 to 145)	20 (44 to 64)	10*	21 (60 to 81)	18 (140 to 158)	
Freq. (GHz)	110	120	130	135	140	135	135	130	44 to 64	77	72	149.9	155.7
P_{SAT} (dBm)	22.7	22.6	22.4	15	17.5	17.6	19.3	21.9	18.5 to 21.5	16.2	21	1.9	1.8
PAE_{MAX} (%)	18.7	17.2	16.1	12.8	13.4	17.5	13	12.5	16.1 to 29	12	13.6	<12*****	<10*****
PAE @ 6-dB PBO (%)	12.1	11.7	9.8	<5*	<5*	8.5	6.7	<5*	9.5 to 17.6	5.7	7	<4*****	<3*****
Modulation Scheme	64-QAM		16-QAM	N.A.	N.A.	N.A.	N.A.	N.A.	64-QAM	64-QAM		16-QAM 8 Channels	64-QAM 8 Channels
Freq. (GHz)	131		131.5	N.A.	N.A.	N.A.	N.A.	N.A.	54	72		CH5: 150.7	CH5: 150.7
Data Rate (Gb/s)	4.8		8	N.A.	N.A.	N.A.	N.A.	N.A.	6	0.6		7.04	10.56
PAPR (dB)	9		8	N.A.	N.A.	N.A.	N.A.	N.A.	7.35	N.A.		N.A.	N.A.
P_{AVG} (dBm)	13.8		13.7	N.A.	N.A.	N.A.	N.A.	N.A.	14.6	15.9		0.1	0.1
PAE_{AVG} (%)	8 (CE) 7.9 (PAE)		7.9 (CE) 7.8 (PAE)	N.A.	N.A.	N.A.	N.A.	N.A.	21 (CE) 16 (PAE)	7.2		0.24 (P_{OUT}/P_{DC})	0.24 (P_{OUT}/P_{DC})
EVM (%)	10.9		11.6	N.A.	N.A.	N.A.	N.A.	N.A.	4.7	5.5		6.8	8
Area (mm^2)	1.11 (0.58**)			0.041**	0.43**	0.18**	0.26**	1.71	1.62	0.1**	0.19**	2.98	

*: Estimated from reported figures. **: Die area not including DC and RF pads. ***: Output stage. ****: Estimated from PA Simulated results

Figure 19.1.6: Performance summary and comparison with prior-art silicon-based mm-Wave PAs/Txs.

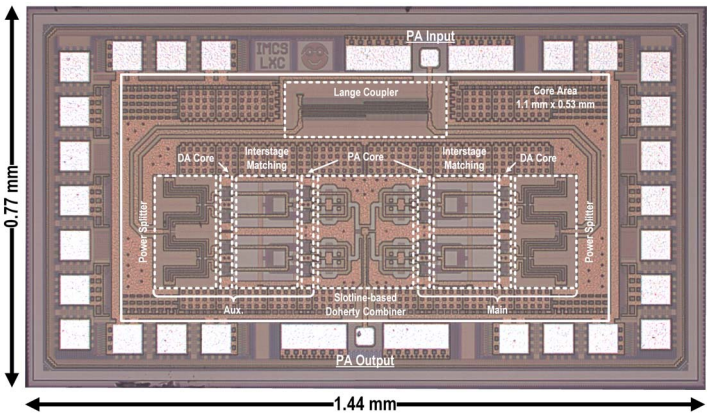

Figure 19.1.7: Die micrograph.

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