4.3 A 140GHz Transceiver with Integrated Antenna, Inherent-Low-Loss Duplexing and Adaptive Self-Interference Cancellation for FMCW Monostatic Radar

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Sub-THz radars in CMOS are attractive in vital-sign and security-sensing applications, due to their low cost, small size, and high resolution. The commonly used bistatic configuration, however, leads to serious beam misalignment between TX and RX, when large-aperture lenses/mirrors are used for longer range and higher spatial precision. As shown in [1], a 4mm physical separation between TX antennas at 122GHz can cause 10° TRX beam misalignment, exceeding the 3dB beamwidth of the 29dB-directivity beam. In the monostatic case, therefore, a reference signal is needed when sufficient TRX isolation is achieved to avoid saturating the RX. Prior monostatic radars [2-6] adopt hybrid/directional couplers for passive TRX duplexing, but at the cost of 3dB+3dB insertion loss inherent to couplers. In [3], such extra loss is mitigated through two sets of hybrid couplers and a quad-feed circularly polarized antenna. Note that in all full-duplex systems, antenna interface mismatch degrades the TRX isolation; in [3], the achieved 26dB isolation relies on excellent antenna matching enabled by backside radiation through a silicon lens. In comparison, frontside radiation allows for low-cost packaging and pairing with compact, large-aperture planar lens, but it causes much degraded antenna matching, hence is challenging for monostatic operation. In this paper, we present a 140GHz monostatic radar in CMOS, which not only circumvents the 6dB inherent insertion loss of couplers, but also facilitates the highly-desired frontside radiation through an adaptive self-interference cancellation (SIC), achieving 33.3dB of total TRX isolation.

The key technique for inherently lossless duplexing is illustrated in Fig. 4.3.1, where a tunable antenna is driven by two feed ports, and . With a 90° delay line in the port path, a common-mode excitation creates a right-handed circularly polarized (RHCP) radiation in the TX mode. When reflected from the target, the wave received by the same antenna becomes left-handed circularly polarized (LHCP), inducing the same relative phase among the four antenna branches as in the TX mode. Interestingly, with the additional 90° delay in the port path, the RX signal is in differential mode at the and ports, and the additional 90° delay in the port path, the RX signal is in common-mode mode at the and ports. Next, to redirect these two mode components to corresponding TX and RX circuits, a compact, dual-slot-based duplexer structure is adopted, where two identical microstrip slots are connected in series at the TX port, and in series at the RX port. As Fig. 4.3.1 shows, signal injection at the TX port leads to , and the CPW-like field distribution in the two slots gives ideally zero leakage at the RX port. Next, when , the electrical potentials in the two slots are summed and extracted at the RX port, but are shorted at the TX port. The simulated TX-ANT and ANT-RX insertion losses, mainly due to metal resistance, are only 0.4dB and 1.6dB, respectively, while the TX-ANT isolation with fully matched antenna ports is 34dB (Fig. 4.3.2). The combination of the duplexer and tunable antenna then enables monostatic operation without 6dB coupler inherent loss. The adopted circular polarization also mitigates radar clutter caused by the second reflection at the ground, since double-reflection will generate the same RHCP wave and thus cannot be received by the RX. Lastly, we note that the above isolation solely relies on structural symmetry of the duplexer; even at extremely large sensing angles (not used in our case), where the wave degenerates to linear polarization, high isolation is still obtained, with only maximum 3dB more inherent ANT-RX insertion loss (Fig. 4.3.1). In simulation, the antenna axial ratio including the degradation from the duplexer structure is below 3dB within 20GHz bandwidth.

The on-chip tunable antenna, shown in Fig. 4.3.2, is based on a crossed hollow bow-tie design, with a PCB metal reflector behind the 150μm-thick Si substrate. Compared to standard crossed-dipole antennas, our design is broadband and the hollow structure minimizes both the blockage of the PCB-reflected wave to the frontside and the coupling to the feed lines, which increases the overall peak radiation efficiency from 19% to 32% (Fig. 4.3.2). To mitigate the isolation degradation caused by antenna mismatch and geometric asymmetry, additional transistors and MOS varactors are connected with the two duplexer mode-balancing devices. With proper differential bias tuning of these devices, a complex signal reflection at the duplexer ANT port is generated to cancel the TX-RX leakage within certain magnitude/phase ranges. Similar to that in [5], the tuning voltages are generated automatically through an adaptive SIC feedback control loop, where the lowpass-filtered RX baseband I-Q signals serve as the indicators for the leakage amplitude and phase. The SIC circuit blocks are given in Fig. 4.3.1. A VGA-based phase tuner is applied to arbitrarily control the sign and phase for the I-Q signals. A second-stage baseband amplifier with off-chip capacitive loads generates an open-loop gain of feedback that is large for a low-IQ leakage signal and small for the high-IQ radar echo signals. Note that a one-time sign control and phase tuning are needed to ensure the negative feedback operation.

Figure 4.3.3 shows the schematics of the RF building blocks. Two +8 multiplier chains are used to turn an input at −17.5GHz to the TX and LO signals at 140GHz. In both the TX and LO paths, 4-stage, two-way power amplifiers (PAs) with slot-based splitter/combiners are adopted, where each stage has a cross-coupled topology for neutralization. The smooth transition from slot to CPW in the splitters/combiners effectively reduces the insertion loss and thus leads to higher RF power output. In simulation, the TX chain has over 11dBm of output power across 18GHz bandwidth. The RX chain includes a low-noise amplifier (LNA) with two cascaded neutralized stages. The simulated gain, noise figure (NF) and power consumption of the LNA including an input noise-matching balun are 11dB, 7.3dB and 6.5dBm, respectively. A trade-off between the LNA gain and its linearity is intentionally applied here, in order to conservatively protect the RX from saturation due to the potential TX to RX leakage. The output of the LNA is connected to two mixers for I-O downconversion. Passive Gilbert mixer topology is chosen to avoid excessive flicker noise that disturbs the SIC loop and lowers the sensitivity. The simulated SSB NF of the LNA+mixer chain is 12dB. Lastly, shown in Fig. 4.3.1, in the I-Q IF paths, highpass filters are inserted before the IF amplifiers for further suppression of the leakage at the IF outputs.

The chip was fabricated using a 65nm bulk CMOS technology. The die micrograph is shown in Fig. 4.3.7. The chip can pair with a detachable planar lens with 39x39mm² size. Realized with 3D polymer and metal printing, the lens has 24x24 metasurface resonator units for local phase-shifting. The measured peak EIRP, with and without the lens, is 25.2dBm and 9.8dBm, respectively. The measured lens-enhanced radiation patterns in Fig. 4.3.4 not only show sharp (~4°) beam profile, but also accurate TX and RX beam steering. The lens is a 3.1mm³ volume and consumes 405mW of power. Lastly, a comparison with state-of-the-art monostatic radar chips is given in Fig. 4.3.6. This work achieves the highest total radiated power, and is the only one that simultaneously mitigates the 6dB inherent coupler loss and reaches >30dB isolation.

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References:
Figure 4.3.1: System diagram and operation principle of the monostatic radar transceiver chip.

Figure 4.3.2: Principle of on-chip antenna with duplexer, adaptive SIC scheme, and simulated performances.

Figure 4.3.3: Schematics of the TX/LO power amplifier (PA), RX low-noise amplifier (LNA), passive mixer and input multiplier chain (×8).

Figure 4.3.4: Photos of assembly and measurement setups, measured TX and RX performances, and radiation patterns of the radar transceiver chip.

Figure 4.3.5: Measured FMCW detection performance and isolation level. Block diagram and photos of the radar detection setup are also shown.

Figure 4.3.6: Comparison with state-of-the-art FMCW monostatic integrated radars.
Figure 4.3.7: Die Micrograph.