4.5 Electronic THz Pencil Beam Forming and 2D Steering for High Angular-Resolution Operation: A 98×98-Unit 265GHz CMOS Reflectarray with In-Unit Digital Beam Shaping and Squint Correction

Nathan M. Monroe[1], Georgios C. Dogiamis[2], Robert Stingel[2], Preston Myers[2], Xibi Chen[1], Ruonan Han[1]

[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Intel Corporation, Chandler, AZ

Ultra-sharp beam forming and high-angular-resolution steering in both azimuth and elevation directions are required in high-performance imaging sensors, spatial-multiplexed wireless links and other applications. This poses great challenges due to the fundamental relationship between the beamwidth and the dimension of the antenna aperture. As shown in Fig. 4.5.1, the aperture size required to achieve 1° of 3dB beamwidth is 0.6×0.6m^2 and 0.2×0.2m^2 at 24GHz and 77GHz, respectively. In current radars, sparse MIMO antenna schemes are adopted to synthesize virtual arrays with the above size in one dimension. However, they require intensive signal processing of many channels. The complex signal routing and placement of active electronics also leads to challenges in the 2D scaling required for pencil beam forming. By increasing the wave frequency to 265GHz, the work in this paper significantly reduces the aperture area, allowing it to be fully realized by digitally controlled, reflective antennas in CMOS microelectronic chips (Fig. 4.5.1). Similar to a concave mirror, a reflectarray, when illuminated by a single radar source, applies incident-angle-dependent phase shifts (e.g. φ_1 and φ_2 in Fig. 4.5.1) to the wave and re-focuses it towards a desired direction. This quasi-optical spatial feed eliminates the high-frequency signal routing and complex processing inherent to MIMO arrays. Employing 98×98 antenna elements, we experimentally demonstrate the forming and electronic steering of a THz pencil beam with ~1° beamwidth in two dimensions. With under-antenna integration of dense memory cells, sidelobe reduction and squint correction are also achieved.

The design of the reflective antenna unit is shown in Fig. 4.5.2. Generally, multi-bit THz phase-shifters in CMOS have large and phase-dependent insertion loss and errors in phase-shift value, degrading radiation performance. Common topologies such as active vector-summing shifters also do not suit dense 2D array integration due to their large footprint and power consumption; their unidirectional operation also does not allow monostatic radar configurations to exploit high-directivity beams in both TX and RX with precise mutual alignment (Fig. 4.5.1). Our design (Fig. 4.5.2) is based on a square patch antenna in the C4 pad layer. It avoids those problems by adopting 1-bit phase-shifting (similar to [1]) and cross-polarization backscattering. The incident wave excites the TM_{010} mode of the antenna and is extracted by a microstrip line tapping at the antenna edge (P1), which connects to a pair of passive FinFET switches. Controlled by gate signal D, the signal is routed to one of the two orthogonal patch edges (P2 or P3), re-radiating the wave with the TM_{100} mode of the antenna. The polarity-flipping design mitigates performance degradation due to interference between the beamformed fields and undesired reflections from passive structures, a problem typical of reflectarrays. Unlike other multi-bit [2] or 1-bit impedance-tuning-based [1] reflect/transmit arrays, this design relies on structural symmetry, producing precise 0°/180° phase inversion and equal amplitude between D=0 and D=1. In simulation, this compact phase-shifting scheme with optimal FinFET sizing (Fig. 4.5.2) gives an insertion loss of 2.7dB. Although 1-bit phase-shifting results in large quantization error, as the calculated radiation patterns in Fig. 4.5.2 show, sharp beams are still formed with large array scale N, due to increased aperture size, coherent addition of fields in the mainlobe, and the spatial feed's randomization of phase-quantization errors.

Compared to prior RF-THz reflect/transmit arrays using discrete phase-shifting devices, our work in CMOS does not require any high-speed control signals from external electronics, due to an 80-kbit shift-register memory integrated under each antenna (Fig. 4.5.3). After a one-time loading of pre-calculated data (Mode 1), the bits in each cell are read out sequentially and cyclically (Mode 2) to control the antenna phase shift for raster-scan imaging. Although in principle beam forming for a radar image only needs 1bit per beam state per antenna (10kbits total per antenna for an example 100×100 pixel image), the extra memory space allows for two additional performance enhancing functions. First, reduction of the sidelobe floor caused by the 1-bit phase-quantization error is enabled by a time-dithering approach [3]. In the pre-calculation for the antenna 1-bit phase data (D_0, D_1…), a time-variant phase offset $\Delta\varphi$ is added to each ideal phase value before 1-bit quantization (Fig. 4.5.3). $\Delta\varphi$ is always uniform across the array, hence not altering the beam direction. However, due to quantization's inherent nonlinearity, a $\Delta\varphi$ changing at each T_{clk} will scramble the quantization sidelobes' magnitude and phase, while adding $\Delta\varphi$ to mainlobe phase. At the receiver, when the signal segments at these T_{clk} are coherently added (by subtracting the corresponding $\Delta\varphi$ via low-frequency LO phase shifting), the scrambled quantization sidelobes add incoherently, leading to an effective sidelobe reduction [3]. Such dithering, although effective, was previously impractical due to the need for ultra-fast data refresh from external electronics. Our architecture enables it, where each memory sector pre-stores and outputs antenna phase data calculated with $\Delta\varphi$=[0°, 45°, 90°, 135°] for a beam steered in a given direction. Secondly, our memory architecture enables the correction of beam squint, which degrades the angular resolution in wideband FMCW imaging radars. Experimental results shown in Fig. 4.5.5 reveal that for a 10GHz sweep, the tilting of beam direction θ exceeds the beamwidth, degrading effective image resolution. Shown in Fig. 4.5.3, our memory design, on top of time dithering, supports squint correction by storing phase values corresponding to different frequencies within an FMCW chirp. Such correction, requiring only synchronization between the low-frequency memory clock and the chirp, is transparent to the external transceiver.

The reflectarray is implemented as a 14×14 tiling of identical 22nm CMOS dies on PCB (Fig. 4.5.4). Each die has an area of 4×4mm^2 and contains 7×7 antenna units. The overall aperture is 58×58mm^2, with ~780Mb built-in memory. An identical pitch of about half wavelength is maintained among antennas both within chip and between adjacent chips. The chips are inter-connected via low-profile bond wires at their edges. Power and phase data are provided from the boundaries of the assembly, and chip-select signals configure each chip to either accept incoming data or pass it onto its neighbors, allowing for high scalability and robustness to potential defective chips with negligible performance degradation. In our experiments, a VDI WR-3.4 source along with a bent waveguide-opening feed is used on a motorized rotation stage. A VDI WR-3.4 sub-harmonic mixer is fixed at a 1.6m distance to test beam-forming patterns. Figure 4.5.5 shows the measured radiation patterns of a 265GHz beam electronically steered to 0°, ±20°, ±40° and ±60°. At boresight, the beam has a directivity of 42dBi and a 3dB beamwidth of 1.0°. The estimated total insertion loss of the in-unit phase-shifter is 3dB. From 260 to 270GHz, a beam squint of ~3° is measured. Our tests show that this effect can be significantly mitigated when corrected phase patterns at 260 and 270GHz are loaded from the integrated memory. The decreased amplitudes at 260 and 270GHz are due to the finite bandwidth of the on-chip patch antennas. In Fig. 4.5.5, sidelobe reduction using dithering is also demonstrated. When based on a static phase pattern, an array-generated beam at -30° possesses a -30 to -35dB sidelobe floor. With 4× time dithering ($\Delta\varphi$=0°, 45°, 90° and 135°), the integrated sidelobe floor from -20° to 80° is decreased by 4.6dB, approaching the case using ideal phase shifters and reducing clutter in imaging applications. At VDD=1V, the static and dynamic current of the entire array, due to the integrated memory, are 150mA and 850mA (f_{CLK}=100kHz), respectively.

The real-world applicability of the presented approaches is demonstrated in an imaging application given in Fig. 4.5.6. For system simplicity, the radar employs the CMOS reflectarray without previously described sidelobe and squint reduction, in a bistatic FMCW (BW=1.92GHz) configuration consisting of a VDI WR3.4 source with +20dBm power and a VDI WR3.4 sub-harmonic mixer with 12dB noise figure. Raster scan with 1° step size reveals the locations of multiple targets, some having an angular offset of only 3°. In addition, a three-dimensional, electronically-scanned radar image of pixels in 1° steps across [-45°, +45°] in both axes detects a number of targets spread across a complex scene. Lastly, Fig. 4.5.6 shows a comparison with state-of-the-art chip-based THz beam-steering arrays, demonstrating this work's superior beamwidth and steering range. In addition to imaging, potential applications of this work also include reconfigurable point-to-point wireless links, relays for non-line-of-sight communications, complex wave-front (e.g. orbital angular momentum) generation, and any application relying on electronically-steered THz pencil beams.

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References:

[1] J. Lynch et al., "Coded Aperture Subreflector Array for High Resolution Radar Imaging". *SPIE*. 2019.
[2] S. Venkatesh et al., "A High-Speed Programmable and Scalable Terahertz Holographic Metasurface Based on Tiled CMOS Chips". *Nature Electronics*, Dec. 2020.
[3] H. Kamoda et al., "Experimental Verification of Novel Method to Reduce Quantization Lobes for Phased Array Radar", *EuRAD*, 2012.
[4] Saeidi et al., "THz Prism: One-Shot Simultaneous Multi-Node Angular Localization Using Spectrum-to-Space Mapping with 360-to-400GHz Broadband Transceiver and Dual-Port Integrated Leaky-Wave Antennas", *ISSCC*, pp. 314-315, Feb. 2021.
[5] H. Jalili et al., "A 436-to-467GHz Lens-Integrated Reconfigurable Radiating Source with Continuous 2D Steering and Multi-Beam Operations in 65nm CMOS", *ISSCC*, pp. 326-327, Feb. 2021.

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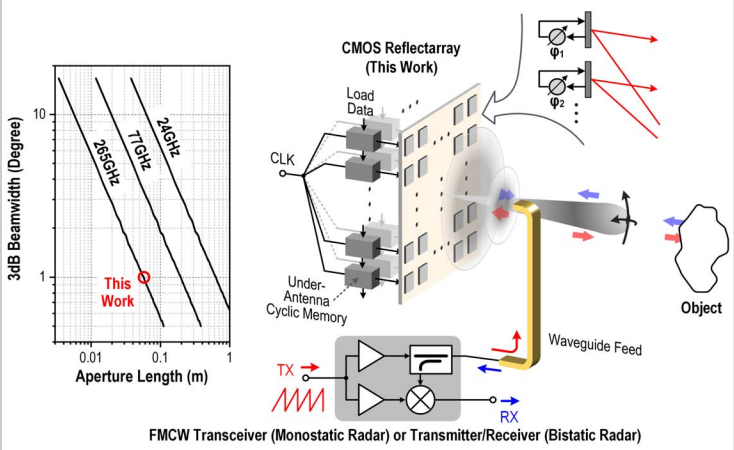


Figure 4.5.1: (Left) Tradeoff between aperture size and beamwidth of beam forming, (Right) architecture and operation of the presented 265GHz CMOS reflectarray.

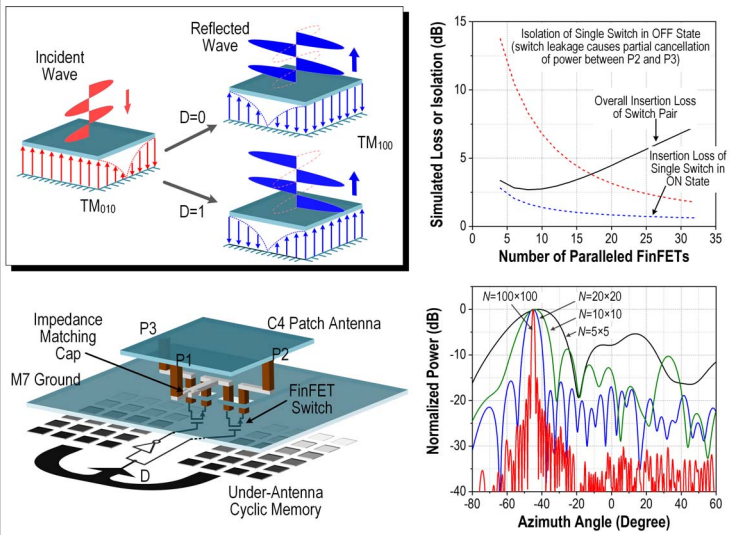


Figure 4.5.2: (Left) Design of the memory-integrated reflect antenna and the 1-bit phase-shifting operation; (Right) simulated performance and the beam-forming patterns of various 1-bit reflectarray sizes, *N*.

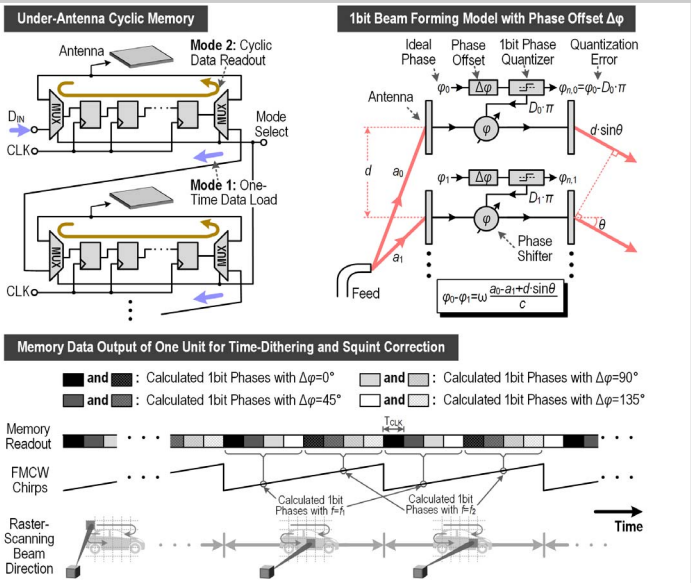


Figure 4.5.3: Sidelobe reduction and squint correction enabled by the under-antenna integrated memory cells.

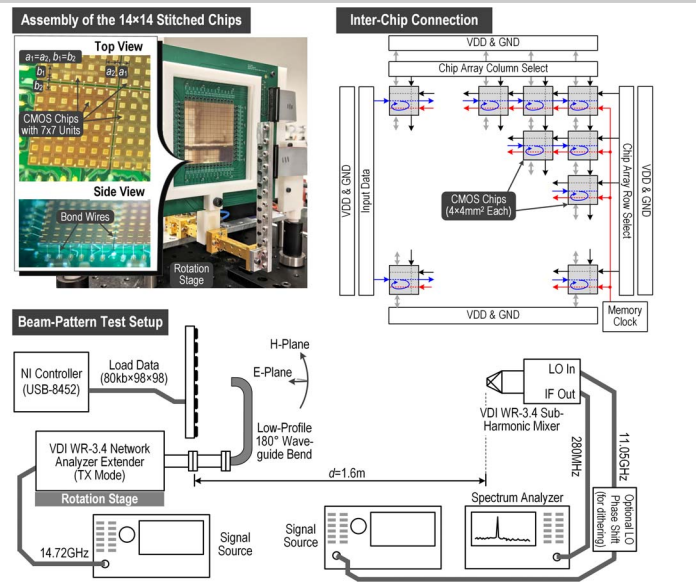


Figure 4.5.4: (Top) assembly and inter-chip connection of the chip array. (Bottom) setup for the beam-pattern measurement.

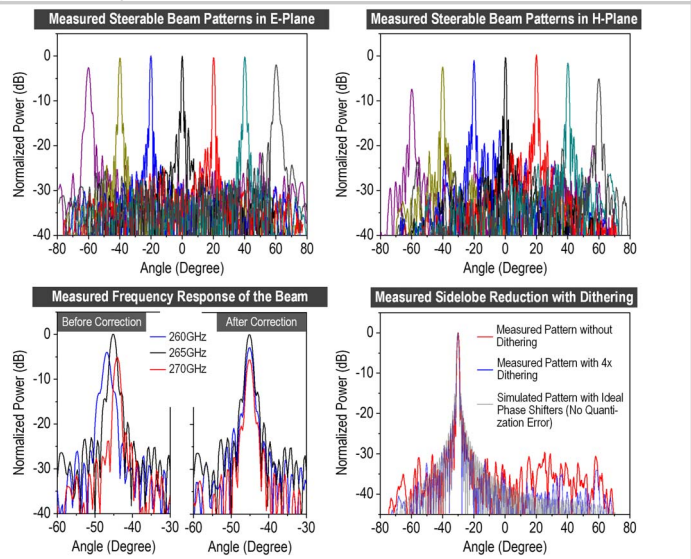
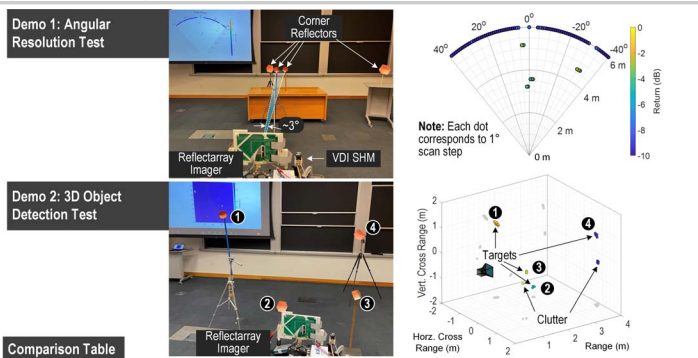


Figure 4.5.5: (Top) Measured radiation patterns of electronically-scanned pencil-beam steering in both E and H-planes. (Bottom) Demonstration of algorithms for beam-squint correction and sidelobe mitigation.



Comparison Table

	Freq. (GHz)	Beam Forming Approach	Array Size	3dB Beam-width	Steering Range	Automatic Beam Profile Correction?	Technology	Area	Power Consumption	3D Sensing Demo?
ISSCC 2021 [4]	380	Active-Driven Beam Squint Antenna	2x1	~15° (1)	±40°	No	65nm CMOS	3mm²	0.14W (TX) 0.16 (RX)	NA
ISSCC 2021 [5]	450	Active Reconfigurable Array+Si Lens	3x7	~7° (2)	±28° & ±8°	No	65nm CMOS	4mm²	0.051~0.095W	
SPIE 2019 [1]	235	Reflect Array (Tiled GaN Chips)	32x32 (3)	~3°	> ±40°	No	GaN + Silicon Micromachining	31mm² (Chip) 500mm² (Array)	NA	
Nat. E. 2020 [2]	300	Transmit Array (Tiled CMOS Chips)	24x24	~10° (4)	±30°	No	65nm CMOS	4mm² (Chip) 16mm² (Array)	0.025W (5) (f_{clk}=5GHz)	
This Work	260	Reflect Array (6) (Tiled CMOS Chips)	98x98	1°	> ±60°	Yes	22nm CMOS	16mm² (Chip) 3100mm² (Array)	0.85W (7) (f_{clk}=100kHz)	Yes

(1) Achieved only in one dimension. (2) Achieved through a Si lens (R=5mm). (3) ~50% of array units not functioning
(4) Estimated from the simulated value control during beam scanning (5) Dynamic power driving phase shifter switches. (6) The only all-inclusive solution requiring no external data
(7) Dynamic power driving 98x98x2 phase shifter switches and 780Mb built-in cyclic memory

Figure 4.5.6: (Top) Imaging demonstration. (Bottom) comparison with the state-of-the-art THz beam-forming chips.

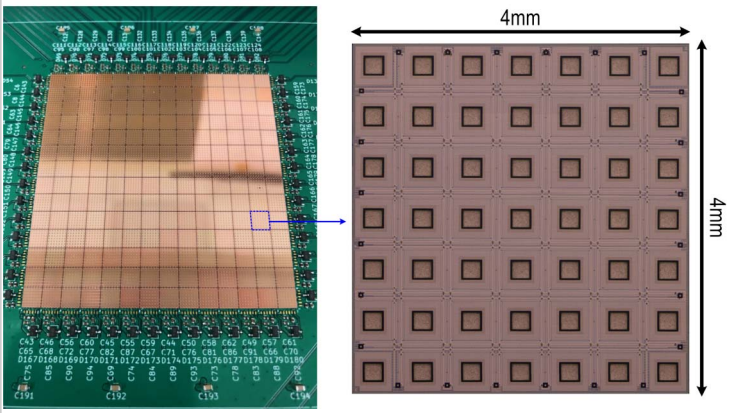


Figure 4.5.7: Photos of the CMOS chip and the array assembly.

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