A Dual-Antenna, 263-GHz Energy Harvester in CMOS for Ultra-Miniaturized Platforms with 13.6% RF-to-DC Conversion Efficiency at -8 dBm Input Power

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***Abstract* — This paper reports a CMOS energy harvester, which operates at so far the highest reported frequency (263 GHz) in order to realize wireless powering of ultra-miniaturized platforms. To maximize the THz-to-DC conversion efficiency, η, at low available radiation power, the harvester not only utilizes a high-speed 22-nm FinFET transistor but also achieves the optimal operating conditions of the device. In specific, the circuit enables self-gate biasing; and through a dual-antenna topology, it drives the transistor drain and gate terminals with both optimal voltage phase difference and power ratio simultaneously and precisely. With a low input power of -8 dBm, the harvester achieves 13.6% measured conversion efficiency and delivers 22 μW to a 1-kΩ load. Without relying on any external component, the harvester chip occupies an area of 0.61×0.93 mm^2.**

***Keywords* — THz, dual antenna, energy harvesting, wireless power transfer, optimum conditions, 22-nm FinFET, self-biasing.**

I. Introduction

Pushing the wave frequency of far-field wireless power transfer (WPT) to the terahertz regime is essential for ultra-miniaturized, battery-less platforms, which currently can only be powered through light or ultra-sound. As an example, the mm^2-size THz identification tag (THz-ID) in [1], [2] relies on integrated photo-diodes, and THz WPT will allow embedding the tags into optically-opaque packages of small-size goods (e.g., semiconductor chips) for authentication and logistic tracking. Previously, the highest harvesting frequency in silicon was only 94 GHz [3], [4]. As shown next, implementation of on-chip THz harvesters requires not only high-speed nonlinear devices, but also unconventional peripheral circuits that maximize the rectification efficiency, η, of the device near its speed limit. It is also noteworthy that prior mm-Wave harvesters [3]–[9] are designed to work with high input power of a few to tens of mW; at sub-mW input level, their efficiencies drop sharply. Such high-power condition is, however, typically infeasible in THz setups. For instance, from a state-of-the-art 0.3-THz III-V source with 20-dBm output and 26-dBi antenna gain, the power received by an on-chip antenna (∼2-dBi gain) at 5-cm distance is only -8 dBm. The corresponding reduced signal swing makes it difficult to fully utilize the device nonlinearity for rectification. In this paper, a 263-GHz energy harvester using Intel's 22-nm FinFET process is reported, increasing the highest frequency of CMOS harvester by ∼3x. The antenna-integrated harvester is ultra-compact (∼0.5 mm^2) and does not rely on any external component. At -8-dBm input power level, 13.6% THz-to-DC efficiency is experimentally obtained, resulting in >20-μW harvested DC power – sufficient even for advanced, power-consuming functions, like cryptography in THz-IDs, and motion of microrobots [10] (Fig. 1).

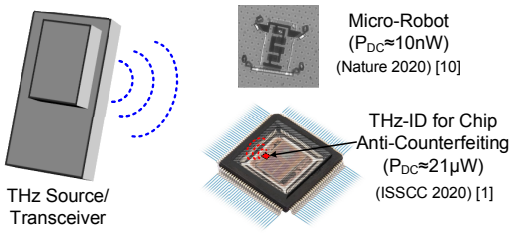

Fig. 1. Applications of THz wireless powering in ultra-miniaturized systems.

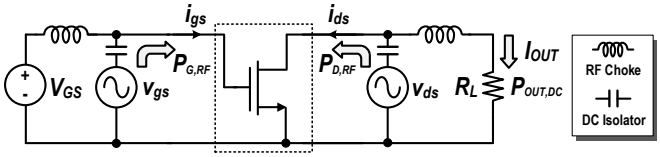

Fig. 2. A generalized testbench for rectification performance test.

II. THz Energy Harvester Design

The THz energy harvester design is presented next with two steps: (1) finding the conditions under which the FET conversion efficiency is maximized, and (2) designing a network around the FET to achieve the above conditions.

A. Optimum Conditions for η_{max}

Although the 22-nm N-FinFET possesses a f_{max} of 450 GHz [11], the closely-spaced thin interconnects connecting to the device inevitably and significantly increase the THz power loss. Efficient THz-to-DC conversion is then only obtained when stringent device operating conditions are met. Fig. 2 shows a generalized testbench to search for such conditions, where two arbitrary RF voltage sources v_{gs} and v_{ds} are driving the gate and drain nodes, respectively, and the rectified DC current I_{OUT} is extracted to a load R_L. The THz-to-DC conversion efficiency is then η=$P_{OUT,DC}$/P_{in}, where the net injected RF power

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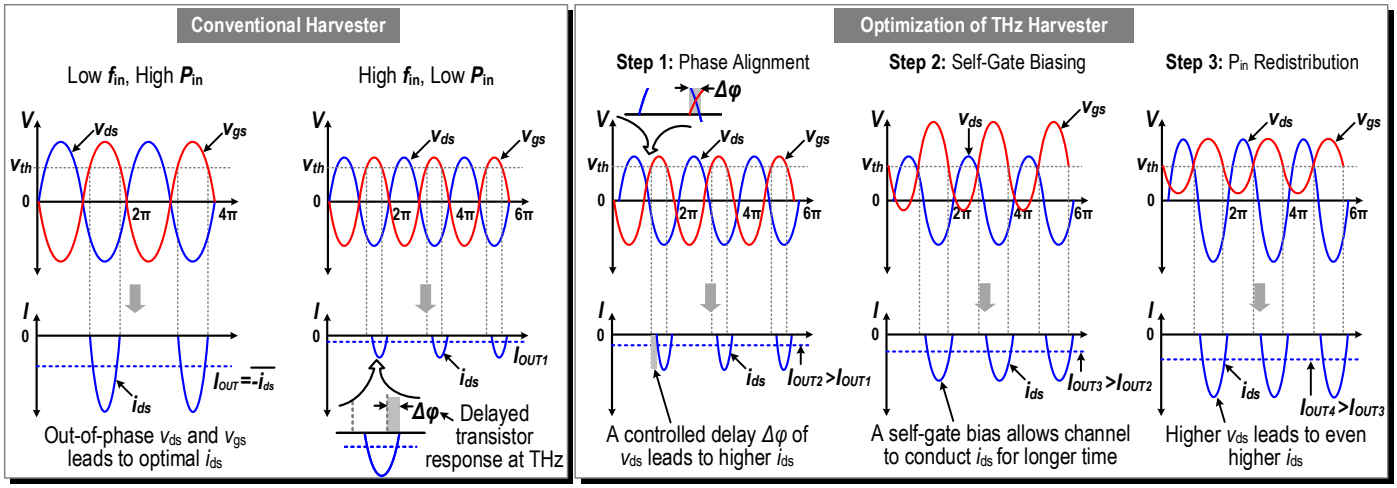


Fig. 3. Rectifying operation of FET in (a) a conventional harvester and (b) our THz harvester with step-by-step optimizations.

P_{in}=$P_{G,RF}$+$P_{D,RF}$=Re $(v_{gs}i_{gs}^*)$+Re $(v_{ds}i_{ds}^*)$. Note that a certain P_{in} corresponds to an infinite number of (v_{gs}, v_{ds}) value sets, and each set gives a different η. Our goal is to find the optimal device driving condition (v_{gs}, v_{ds}) for maximum η. In conventional low-frequency rectifiers, out-of-phase gate and drain voltages are applied (left of Fig. 3a), so that when v_{gs} turns on the channel, a negative v_{ds} reaches its peak simultaneously and creates the maximum i_{ds}, hence the maximum, positive I_{OUT} from the clipped i_{ds} waveform. At THz frequencies, the above conditions are no longer valid. As illustrated in the right of Fig. 3a, the finite pico-second-level transit time of carriers causes a phase delay $\Delta\varphi$ between v_{gs} and the moment the channel is ON. Therefore, if v_{ds} is still out-of-phase with v_{gs}, the channel will be turned OFF prematurely, resulting in an under-driven i_{ds}. For low input THz power P_{in} (hence smaller v_{gs} swing), this under-drive problem is worsened due to shorter channel ON time.

To improve rectification efficiency, a $\Delta\varphi$ delay can be applied to v_{ds} ("Step 1" in Fig. 3b), so that peak v_{ds} and minimum channel resistance occur simultaneously, hence higher i_{ds}. Next, the rectifier DC output voltage can be used to self-bias the transistor gate ("Step 2"), so that the channel is turned ON for a longer duty cycle, further increasing I_{OUT}. Self-biasing also relaxes v_{gs} swing requirement, allowing more P_{in} to be injected to the drain ("Step 3") and causing even higher i_{ds}. The above optimum conditions give the maximum possible efficiency η_{max}. In Fig. 4, a self-biased N-FinFET is simulated with various (v_{gs}, v_{ds}) combinations while keeping P_{in}=-8 dBm. An η_{max} of 25.8% is obtained, when the above $\Delta\varphi$ is $\Delta\varphi_{opt}$=45° and the amplitude ratio $|v_{ds}|/|v_{gs}|$ is A_{opt}=3.75. That corresponds to an input power ratio (m=$P_{D,RF}/P_{G,RF}$ in Fig. 2) of m_{opt}=2.2. Fig. 4 also shows that even with losses of peripheral passives (to be designed next), the above conditions still lead to η_{max}=15%. Note that no prior reported work meets all those conditions.

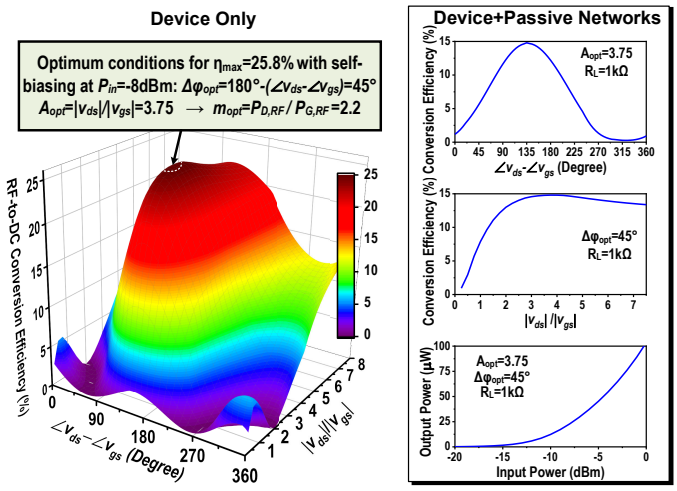


Fig. 4. Simulated rectification performance of a N-FinFET (8×270nm/22nm) at various v_{ds} and v_{gs} ratio and phase difference. The inset shows the simulated results including the losses from device vias and matching networks.

B. *Circuit for Optimum Conditions: A Dual-Antenna Design*

Conventional harvester topologies adopting a single antenna or uniform antenna array (Fig. 5) are not appropriate for THz operations; because it is difficult to create a passive network between the antenna and the transistor, which simultaneously achieves the above ($\Delta\varphi_{opt}, m_{opt}$) conditions and the conjugate matching at both the gate and drain nodes. The complexity of such a network also normally incurs large power loss. Our harvester adopts a compact scheme (Fig. 5) involving two asymmetric patch antennas driving the gate and drain separately. This dual-antenna topology corresponds to a systematic design flow:

1) While the antenna length determines the resonance frequency, the width being proportional to the radiation aperture has a near linear relation with the antenna gain (see Fig. 6b). Given the uniform power density

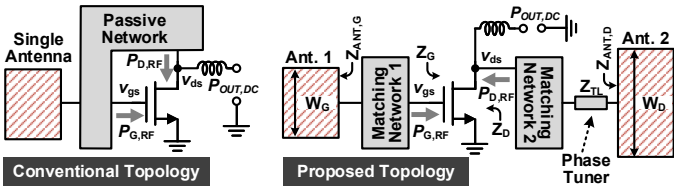


Fig. 5. Comparison between the conventional single-antenna topology and our dual-antenna topology.

of the incident plane wave, the received power ratio of two antennas is then well controlled by the patch width ratio. In our design, by choosing W_G=230 μm and W_D=500 μm, the ratio (m) of power injected into the device nodes is readily fixed at m_{opt}=2.2.

2) Now, the matching networks for gate and drain are decoupled and only need to transform Z_G and Z_D in Fig. 5 to the two antenna impedances $Z_{ANT,G}$ and $Z_{ANT,D}$, respectively. Here, Z_G and Z_D are the *active impedances* of the gate and drain, and are derived by Z_G=v_{gs}/i_{gs} and Z_D=v_{ds}/i_{ds} in Fig. 2, when the simulated device is driven under the optimal conditions.
3) Finally, to achieve $\Delta\varphi_{opt}$, a transmission line (TL) is inserted between the antenna and matching network on the drain side[1] (Fig. 5). The length of the TL is then adjusted until $\Delta\varphi_{opt}$ is met at the device drain and gate[2].

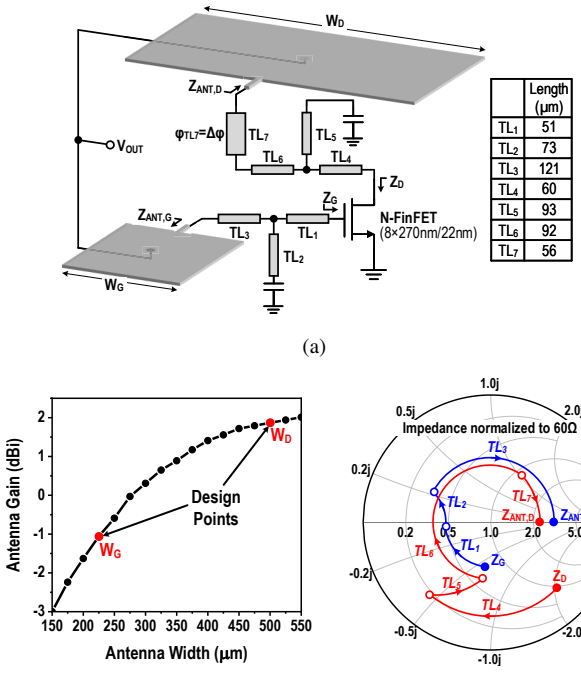
The schematic based on the above flow is shown in Fig. 6a. The adopted multi-stub matching networks ($TL_{1,2,3}$ and $TL_{4,5,6}$) along with the impedance transformation details given on a Smith chart are shown in Fig. 6c. The additional phase tuning is provided by TL_7. Lastly, connecting the central AC ground nodes of the patch antennas together enables self-biasing of the transistor without interfering with antenna operations. Such a scheme also ensures that the self-bias voltage is close to the transistor V_{th}=0.18 V when driving an optimum load (see Fig. 8a). The same connection is also used to extract DC output power, thus avoiding lossy RF chokes.

III. Measurement Results

The chip is fabricated in a 22-nm FinFET process and has an area of 630×910 μm^2 as shown in Fig. 7a. Most of the silicon and bottom metal layers under and around the antennas are unused and can be utilized for added functionality in future systems. The measurement setup is shown in Fig. 7b, where a VDI amplifier-multiplier chain (AMC) radiates 90-mW 263-GHz signal with a 26-dBi horn antenna, and a digital multimeter measures the output voltage across a variable load resistor. The output power of AMC is measured using

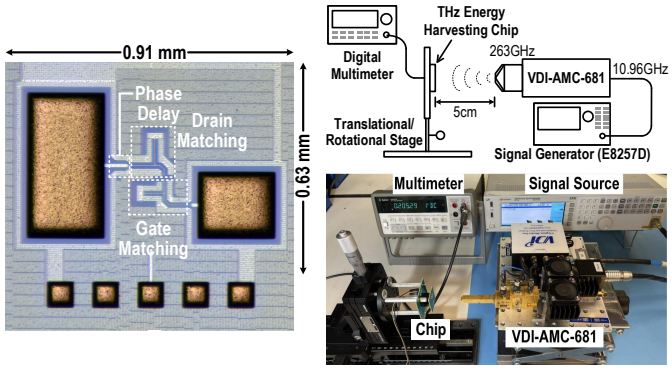
[1]This assumes additional phase delay on the drain side is needed. Note that the opposite orientations of the antennas provide an extra 180° phase between v_{gs} and v_{ds}; that eliminates the need of a lossy transformer or balun to approach $\angle v_{ds}$-$\angle v_{gs}$=180°-$\Delta\varphi_{opt}$=135°.

[2]Ideally, the TL impedance Z_{TL} is set to be the same as $Z_{ANT,D}$, so that its length adjustment does not affect the matching from the previous step. If $Z_{ANT,D}$ is too high for the phase-tuning TL to realize (our case), a TL with lower Z_{TL} can be used and co-designed with Matching Network 2 in Fig. 5.



(a) (b) (c)

Fig. 6. (a) Schematic of the THz energy harvester. (b) HFSS-simulated antenna gains for different antenna widths. (c) Gate and drain impedance matching networks on a Smith chart.

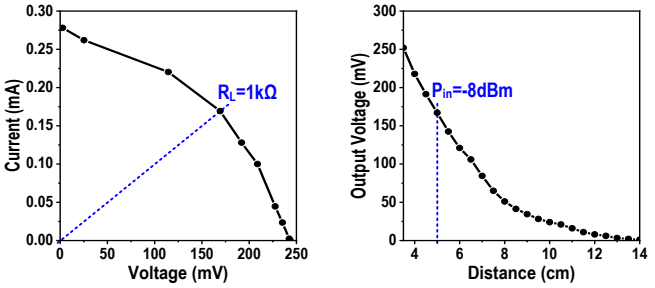


(a) (b)

Fig. 7. (a) Chip micrograph. (b) Diagram and photo of the test setup.

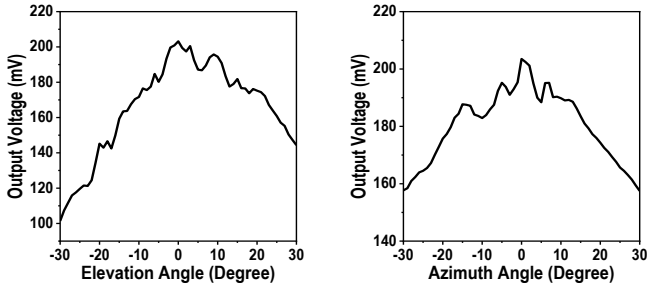
a PM5 Erickson power meter and is also verified with the manufacturer calibration datasheet. The power received by the harvester is calculated using the Friis equation and the simulated gain of on-chip patch antennas.

The measured load line performance of the harvester at 5-cm distance, shown in Fig. 8a, results in an optimum load of ∼1 kΩ. The measured output voltages at various distances are given in Fig. 8b. In Fig. 9, the measured incident angle sensitivity of the harvester is presented. The harvester is more sensitive in the E-plane than in the H-plane, because a non-zero incident angle in the E-plane introduces additional phase shift between the two antenna outputs, causing deviation from the optimum device conditions. For angle-insensitive application scenarios, the two antennas should be closely placed, whereas



(a) (b)

Fig. 8. Measured (a) load line and (b) open-circuit voltage of the harvester.



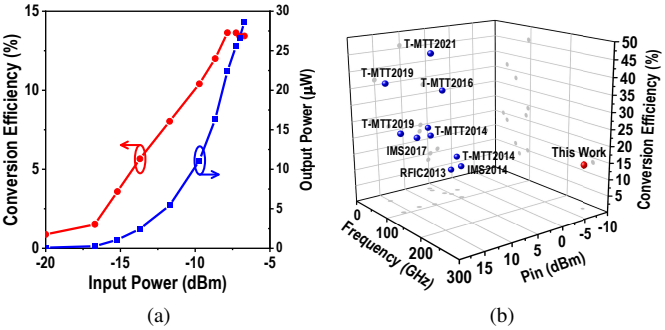
(a) (b)

Fig. 9. Measured angle sensitivity in (a) E- and (b) H-planes.

when high angle sensitivity is desired (e.g., for robustness against undesired beam interrogation), the antennas should be separated apart. Fig. 10a shows the measured efficiency η and $P_{OUT,DC}$, excluding the antenna loss, at various attenuated input power levels. At P_{in}=-8 dBm, η_{max} of 13.6% and $P_{OUT,DC}$ of 22 μW are obtained.

IV. Conclusion

A dual-antenna based 263-GHz energy harvester is presented in 22-nm CMOS process. This work is compared with the state-of-art mm-Wave harvesters in Fig. 10b and in Table 1. It achieves not only the highest harvesting frequency but also a highly competitive conversion efficiency of 13.6% at low input power levels. This is enabled by an antenna-device co-design approach that simultaneously achieves the device optimum conditions under a self-gate biasing. The ultra-compact harvester (~0.5 mm^2) also demonstrates the feasibility of wirelessly powered, package/battery-less systems with the sub-mm^2 form factor.



(a) (b)

Fig. 10. (a) Measured η and $P_{OUT,DC}$ with 1-kΩ load. (b) Comparison of this wok with the state-of-art mm-Wave energy harvesters.

Table 1. Comparison with State-of-Art mm-Wave Energy Harvesters

	CMOS Technology	Freq. (GHz)	Peak Efficiency η_{max}† and Related P_{in}	η at Reduced P_{in} (≤0 dBm)†	Area (mm^2)
This Work	22nm FinFET	263	13.6% at -8dBm	13.6% at -8dBm	0.57
[3]	40nm Bulk	94	45.8% at 10dBm	5% at 0dBm*	0.08#
[4]	65nm Bulk	94	24% at 16dBm	2% at 0dBm*	0.09#
		35	36.5% at 15dBm	10% at 0dBm*	0.12#
[5]	40nm Bulk	60	32.8% at 5.7dBm	10% at -3dBm*	15600‡
[6]	65nm Bulk	24	20% at 6.4dBm	2% at -3dBm*	0.27#
		35	18% at 6.6dBm	4% at 0dBm*	
		60	11% at 3dBm	6% at 0dBm*	
[7]	65nm Bulk	89	21.5% at 12.7dBm	1% at 0dBm*	0.12#
[8]	65nm Bulk	94	10% at 4.5dBm	4% at -2.3dBm*	0.48
[9]	65nm Bulk	71	8% at 5dBm	-	1.8

†Without antenna loss *Estimated from the plots in the literature
#Area without antenna ‡Area including a grid antenna

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