A Sub-THz CMOS Molecular Clock with 20 ppt Stability at 10,000 s Based on Dual-Loop Spectroscopic Detection and Digital Frequency Error Integration

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***Abstract* — This paper presents a dual-loop chip-scale molecular clock (CSMC), which enhances the Allan Deviation performance by combining high signal-to-noise ratio of using fundamental mode and long-term stability of using higher order modes in derivative molecular absorption spectroscopy. In addition, digital frequency-error integration is adopted in the frequency-locked loop to provide an infinite open-loop DC gain, which fully suppresses any frequency drift caused by the temperature-sensitive crystal oscillator. This new generation CSMC is implemented in 65-nm CMOS, and achieves 20 ppt (part-per-trillion) Allan Deviation at 10,000 s averaging time with 71-mW power consumption.**

***Keywords* — frequency stability, dual loop, molecular clock, CMOS, terahertz, spectroscopy, carbonyl sulfide**

I. Introduction

Miniaturized frequency references with high stability are crucial for applications that require precision timing on platforms with stringent constraints on size, weight, and power. Examples include mobile GPS-denied positioning, navigation, high-speed wireless networking, etc. Recently, chip-scale molecular clocks (CSMCs) emerges as a low-cost, CMOS-compatible alternative to chip-scale atomic clocks (CSACs), which requires sophisticated electro-optical spectrometer and thermal-stabilized packaging to interrogate hyperfine transitions of ^{133}Cs or ^{87}Rb atom vapor [1], [2]. Using a CMOS sub-THz spectrometer and a frequency-locked loop (FLL), a recent CSMC delivers a stability (quantified as Allan deviation σ) of 43 ppt at 1000-s averaging time (τ) by referencing to the rotational transition of gaseous carbonyl sulfide (^{16}O^{12}C^{32}S), which has 231.061-GHz center frequency and <1-MHz linewidth [3]. However, the single loop and prior design of servo in [3] has weak frequency regulation against rapid external disturbance, and also deviates from the actual OCS transition line center in the long term, causing more susceptibility to environmental variations. This paper presents a dual-loop CSMC architecture with a digital error integration/correction scheme, which extends frequency regulation from ∼0.01 s to 10,000 s and demonstrates stability improvement over the prior work [3].

II. Challenges in the Previous CSMCs

Previous molecular clocks [3], [4] adopt the architecture in Fig. 1a, which consists of a transmitter (TX), a receiver (RX), and a hermetically-sealed OCS gas cell. In the TX, a probing signal is generated by a PLL referenced to a MHz-level voltage-controlled crystal oscillator (VCXO), and is frequency-modulated (FM) at sub-MHz f_m around its center frequency (f_c) near 231 GHz (Fig. 1b). A THz square-law detector in the RX then detects the signal power that is partially absorbed by OCS and is fluctuating at f_m. Finally, a lock-in detector is used to generate a "frequency-error" signal $V_{LK,N}$ based on the amplitude of either the fundamental (f_m) or odd harmonic component ($N_{odd}{\cdot}f_m$) of the THz detector output (Fig. 1b). With the low-pass-filtered $V_{LK,N}$ controlling the VCXO, f_c dynamically tracks the zero-crossing frequency ($f_{0,N^{th}}$) of the dispersion curve[1], which ideally is the same as the invariant OCS transition frequency f_0. The clock output from the VCXO is therefore stabilized. This architecture, however, still has two major problems.

First, the most recent clock in [3] uses 3^{rd}-order spectral probing (N=3), of which the dispersion curve is less susceptible to any non-flat frequency response of the system, and therefore has higher symmetry (Fig. 1b). That leads to less error and temperature sensitivity of the zero-crossing point [3], hence improved long-term stability. It, however, degrades the short-term (τ<10 s) stability due to the following reason. Theoretical limit of σ is expressed as: $\sigma{=}V_n/(K_r f_0\sqrt{2\tau})$, where K_r and V_n are the slope [V/Hz] and noise voltage at the zero crossing of the dispersion curve. It is noteworthy that the slope K_r in 3^{rd}-order probing is 1.8× lower than in 1^{st}-order probing (see Fig. 1b and 7a), and the corresponding short-term stability is inferior than that of a free-running VCXO. As a design trade-off, the FLL in [3] adopts a closed-loop bandwidth of ∼0.1 Hz, so that frequency regulation based on the 3^{rd}-order spectral probing takes place only for τ>10 s, and the Allan Deviation at τ<10 s is close to that of a free-running VCXO (Fig. 1c). That leaves the clock unprotected against rapid external disturbance to VCXO, such as vibration.

The second problem of the previous clock [3] lies in that, at the zero-crossing point of the odd-order dispersion curve, the even-order harmonic ($N_{even}\ f_m$) components at the THz detector output reach their maximum (Fig. 1b). To avoid receiver saturation, the subsequent signal amplification gain, hence the entire FLL feedback-control loop gain A_{FLL}, is

[1]A dispersion curve is obtained by recording $V_{LK,N}$ when sweeping f_c. The 1^{st}-, 2^{nd}-, and 3^{rd}-order dispersion curves are plotted in Fig. 1b.

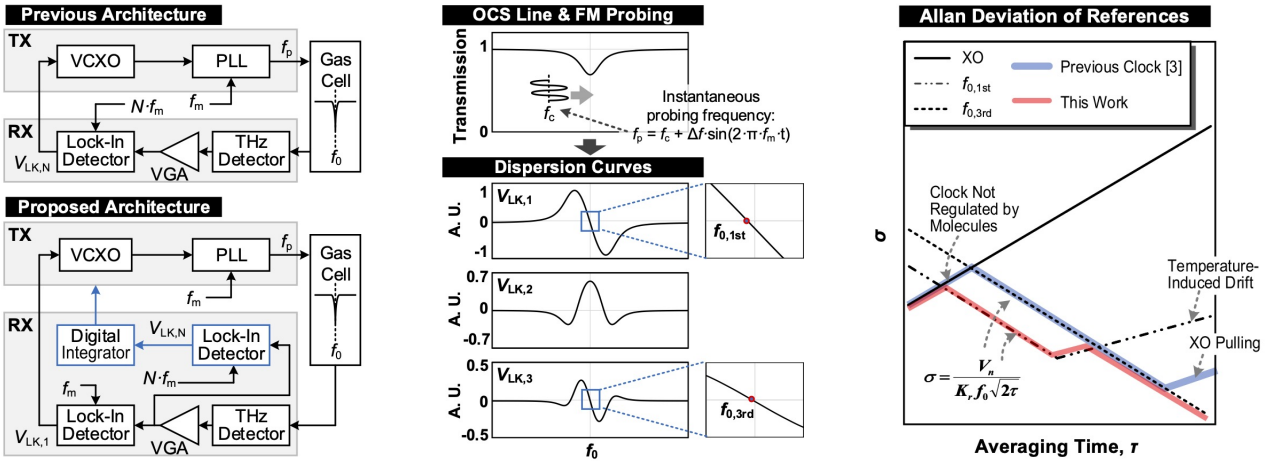


Fig. 1. (a) Comparison of the prior and proposed CSMC architectures. (b) Frequency-modulated probing of the OCS transition line, and corresponding 1^{st}-, 2^{nd}- and 3^{rd}-order dispersion curves. (c) Allan deviation of molecular clocks set by $\sigma{=}V_n/(K_r f_0\sqrt{2\tau})$ from 1^{st}- and 3^{rd}-order spectral probing.

limited. Given the large temperature coefficient ($>10^{-7}$/°C) of the low-power VCXO (0.4 mW) and the long-term environmental temperature drift, the large VCXO drift even after the suppression (by a factor of A_{FLL}) from the molecular frequency-locked loop still exceeds the noise-limited stability $\sigma{=}V_n/(K_r f_0\sqrt{2\tau})$ (i.e. "XO pulling" in Fig. 1c). In [3], with τ=10,000 s, the VCXO output exhibits a drift of $\sim 10^{-7}$, which increases the final instability to $8.8{\times}10^{-11}$ even after a 2^{nd}-order polynomial output frequency compensation.

III. Circuit Details of Our Molecular Clock

Fig. 2 shows a detailed block diagram of the proposed CSMC. The TX consists of two cascaded PLLs, two frequency doublers, and a slot array coupler (SAC). A multi-modulus divider (MMD) with a 36-bit delta-sigma modulator (DSM) is used in both PLLs. From a 26-MHz VCXO, the first PLL (PLL1) generates a 200-MHz clock output (CK_{OUT}) as the reference clock of the second PLL (PLL2) with a 57.77-GHz output. A divide-by-3 frequency divider generates a 66.7-MHz clock for a sine modulator, which provides an 8-bit digital sine wave at f_m=111 kHz and three clock signals at f_m, $3f_m$, and $40f_m$. For frequency modulation of the spectral probing signal, the frequency control word (FCW) of PLL2 (FCW_2) is created by adding the 8-bit word of sine wave to the nominal FCW of PLL2 (FCW_2'). The THz probing signal is generated by a frequency quadrupler following PLL2, and coupled into/out of the waveguide gas cell through an SAC [3] to probe the transition line at 231.0609 GHz. The THz signal is detected by an SAC-fed, MOSFET-based square-law detector, followed by a variable gain amplifier (VGA).

To address the short-term instability explained in Section II, our CSMC adopts an FLL based on *both* the 1^{st}-order and 3^{rd}-order spectral probing (see a comparison in Fig. 1a). While the 1^{st}-order probing forms the main loop with a high SNR enabling effective regulation of short-term instabilities, the 3^{rd}-order probing is used in an auxiliary loop to respond against long-term variations. Such a dual-loop

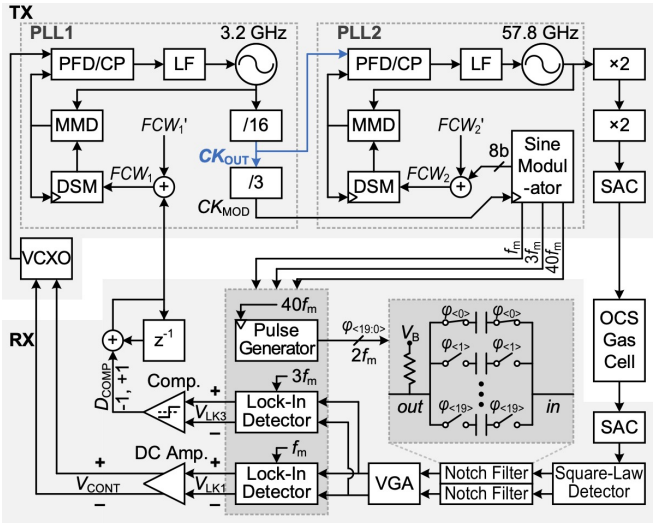
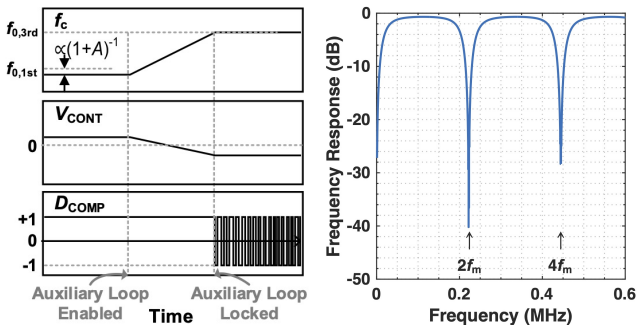


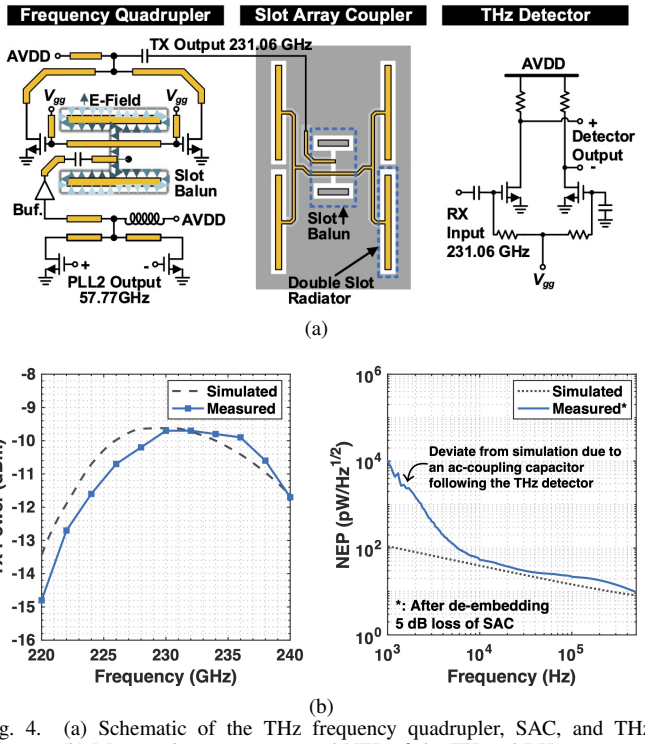
Fig. 2. Block diagram of the proposed CSMC.

scheme is based on two lock-in detectors driven by the f_m and $3f_m$ clocks, respectively. The first lock-in detector in the main loop is followed by a DC amplifier to control the frequency of the VCXO. The output of the second lock-in detector in the auxiliary loop is digitized by a comparator and is then digitally integrated. The integrator output is added to the nominal FCW of PLL1 (FCW_1). The 200-MHz output (3.2GHz÷16) of PLL1 is then jointly adjusted by the 1^{st}-order and 3^{rd}-order spectral probing, and serves as the overall clock output. Within a short time scale (τ<10 s), the weight of frequency control from the 1^{st}-order path (with a constant analog gain) dominates, and provides a high-SNR correction to any fast-changing clock output error. With a longer time scale (τ>100 s), the control from the 3^{rd}-order path, after sufficiently long integration, dominates and performs temperature-insensitive regulation to any slow-varying clock output drift. Fig. 3a shows the clock initialization process with a simplified timing diagram. When the auxiliary loop



(a) (b)

Fig. 3. (a) Timing diagram of the dual-loop locking. (b) Simulated transmission frequency response of the 20-path notch filter.



(a)

(b)

Fig. 4. (a) Schematic of the THz frequency quadrupler, SAC, and THz detector. (b) Measured output power and NEP of the TX and RX.

is enabled, FCW_1 keeps increasing or decreasing until the long-term average of f_c is locked to $f_{0,3^{rd}}$. In the steady state, the comparator keeps toggling with zero averaged output. The digital integration and its infinite equivalent DC gain in the 3^{rd}-order auxiliary loop also ensure that the XO pulling effect described in Section II is fully suppressed. It is noteworthy that the input offset voltages of the DC amplifier and the comparator in the two loops are still translated to the frequency error of the clock, so a large gain of the VGA preceding the lock-in detectors is still desired. In order to suppress the aforementioned, large even-order harmonic components at the VGA input (Fig. 1b), a differential pair of 20-path notch filters are used. Using the $40f_m$ clock from the sine modulator, a pulse generator generates 20 non-overlapping clocks at $2f_m$ ($\varphi_{<i>}$, i=0,1...19 in Fig. 2, which drive the switches in the notch filters. Shown in Fig. 3b, the simulated insertion loss at

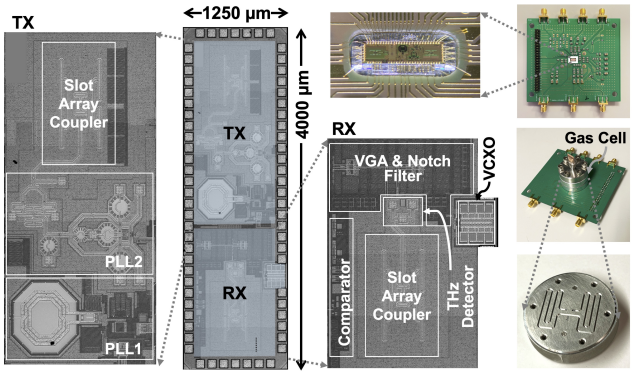
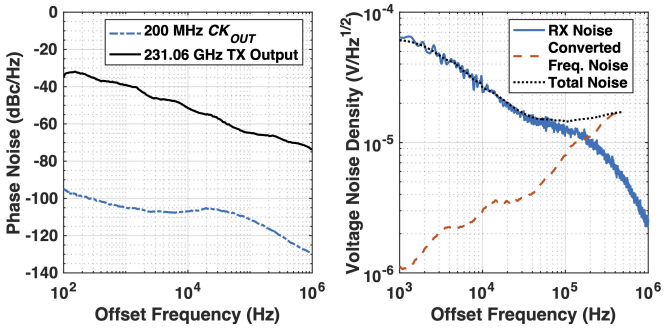


Fig. 5. Chip micrograph and packaging.



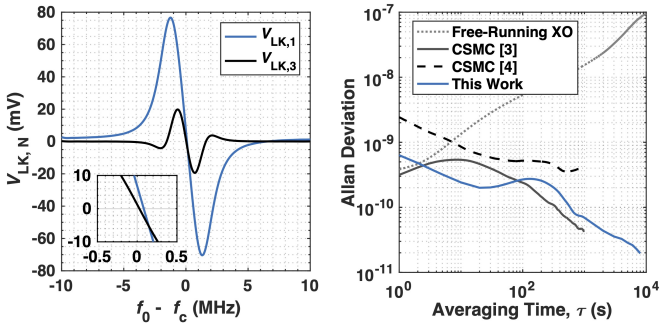
(a) (b)

Fig. 6. (a) Measured phase and frequency noise of the 231.06-GHz probing signal. (b) Measured RX noise at VGA output and the estimated total noise.

f_m and $3f_m$ is ~0.7 dB, and that at $2f_m$ and $4f_m$ is larger than 40 dB and 28 dB, respectively. Lastly, schematics of a few THz blocks are shown in Fig. 4a. The 231-GHz doubler is based on a slot balun input and has a peak simulated output power of -4.4 dBm. To couple the wave from the chip to the waveguide gas cell, a 2×2 slot array is used to focus the beam towards the waveguide opening at the chip back. 5 dB of simulated insertion loss is obtained without relying on any external component. The THz MOSFET detector has a simulated responsivity of 12.2 kV/W and noise equivalent power (NEP) of 13.9 pW/Hz$^{1/2}$ at f_m.

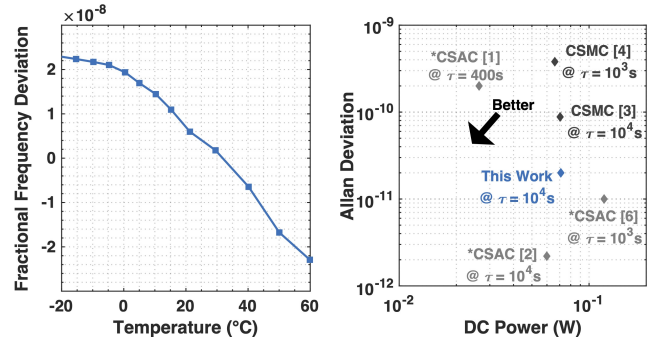
IV. Measurement Results

The chip fabricated in a 65-nm CMOS process consumes 71 mW of power and occupies 5 mm^2 of area. The clock package, including a meandering metal waveguide with 75-mTorr OCS gas sealed inside, is shown in Fig. 5. The measured TX power and RX NEP, shown in Fig. 4, well match the simulation. Shown in Fig. 6a, the measured phase noise of the 231-GHz TX output is -65 dBc/Hz at $2f_m$ offset, and the phase noise of the 200-MHz CK_{OUT} is -129 dBc/Hz at 1-MHz offset. Due to the inter-modulation effect of line probing, the frequency noise of TX output (Fig. 6a) at even order harmonics of f_m is converted to the THz detector output at f_m [5]. Fig. 6b shows such PM-to-AM converted noise, the low-pass-filtered RX noise, and the total noise. Based on these plots, our selected value of f_m (111 kHz) leads to the optimal spectroscopic SNR.



(a) (b)

Fig. 7. (a) Dispersion curves measured by the clock chip. The center frequency of the plot is close to 231.060983 GHz. (b) Measured Allan Deviation.



(a) (b)

Fig. 8. (a) Fractional frequency deviation over temperature variations. (b) Allan Deviation of high stability clocks including CSACs (* in the figure) with high-cost implementations.

Next, using the clock spectrometer configured in an open loop, dispersion curves are measured and shown in Fig. 7a. The measured slopes of the fundamental and 3^{rd}-order dispersion curves are 8.26×10^{-8} V/Hz and 4.51×10^{-8} V/Hz, respectively. Then, after closing the FLL loop, the clock successfully locks onto the molecular transition, and Fig. 7b shows the measured Allan deviation of the clock 200-MHz output. With the 1^{st}-order locking in the main loop, the CSMC achieves σ=5.37×10^{-10} at τ=1 s. Although the CSMC in [3] has a slightly better Allan deviation at 1 s, as explained in Section II, it relies on the stability of the free-running VCXO and is susceptible to rapid environmental disturbances. In comparison, our CSMC provides molecular regulation starting at a much shorter time scale (∼0.01 s), hence is protected against external disturbance causing large VCXO shift. Also, due to the stable 3^{rd}-order locking and digital integration with infinite DC gain, the time averaging of Allan deviation continues up to 10,000 s, and σ=2×10^{-11} is obtained without any temperature compensation. In comparison, the significant XO-pulling effect in [3] requires post temperature compensation, with which the instability is still 4× higher than this work. Lastly, the slight hump in the Allan deviation curve around 200 s can be reduced in the future by having an earlier transition from the main loop to the auxiliary loop as τ grows.

Fig. 8a shows the measured temperature sensitivity of the CSMC. Over the temperature range of -20°C to 60°C, the frequency variation is less than $\pm2.3\times10^{-8}$, resulting in an average temperature coefficient of 5.8×10^{-10}/°C. In [3], the frequency drift over a temperature range of 27°C–65°C is $\pm5.4\times10^{-8}$ without temperature compensation, which corresponds to an average temperature coefficient of 2.8×10^{-9}/°C, about 5× higher than that in this work. Fig. 8b shows a comparison with other high-stability miniaturized clocks: this work achieves the best long-term Allan deviation among CSMCs while consuming similar DC power. A comparison with other CSMCs and CSACs is shown in Table 1.

Table 1. Comparison of High-Stability, Miniaturized Clocks

		[1]	[2]	[6]	[4]	[3]	This Work
Frequency Reference		Ground-State Hyperfine Transition of Atoms*			Rotational Transition of Molecules		
		^{87}Rb	^{133}Cs		$^{16}O^{12}C^{32}S$		
Probing Freq. (GHz)		3.417	4.596		231.061		
Order of Locking		N/A			1^{st}	3^{rd}	1^{st}+3^{rd}
ADEV (10^{-10})	τ = 1s	4	0.67	3	24	3.2**	5.4
	τ = 10s	1.2	0.6	1	8.6	5.4	2.4
	τ = 10^4s	2***	0.05	N/A	N/A	0.88	0.2
Average Temp. Coeff. (10^{-10}/°C)†		N/A	0.07††	0.125††	N/A	28†††	5.8†††
DC Power (mW)		26‡	60	120	66	70	71

*High-cost implementation, **The clock is unlocked at τ=1s, ***At τ=400s,
†Defined as (Temperature-induced frequency drift)/(Temperature range),
††With ovenized temperature stabilization and back-end compensation,
†††Without temperature compensation,
‡The power of the physics package and signal processing is not included.

V. Conclusion

In this paper, we present a dual-loop CSMC with digital frequency-error integration and correction, which breaks the previous trade-offs in 1^{st}- and 3^{rd}-order probing and effectively enhances the robustness and stability of the clock. This work reduces the performance gap of CSMCs with respect to chip-scale atomic clocks, while keeping its advantages in cost, complexity, and power consumption.

Acknowledgment

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