BA759-315

A Dual-Antenna, 263-GHz Energy Harvester in CMOS for Ultra-Miniaturized Platforms with 13.6% RF-to-DC Conversion Efficiency at -8dBm Input Power

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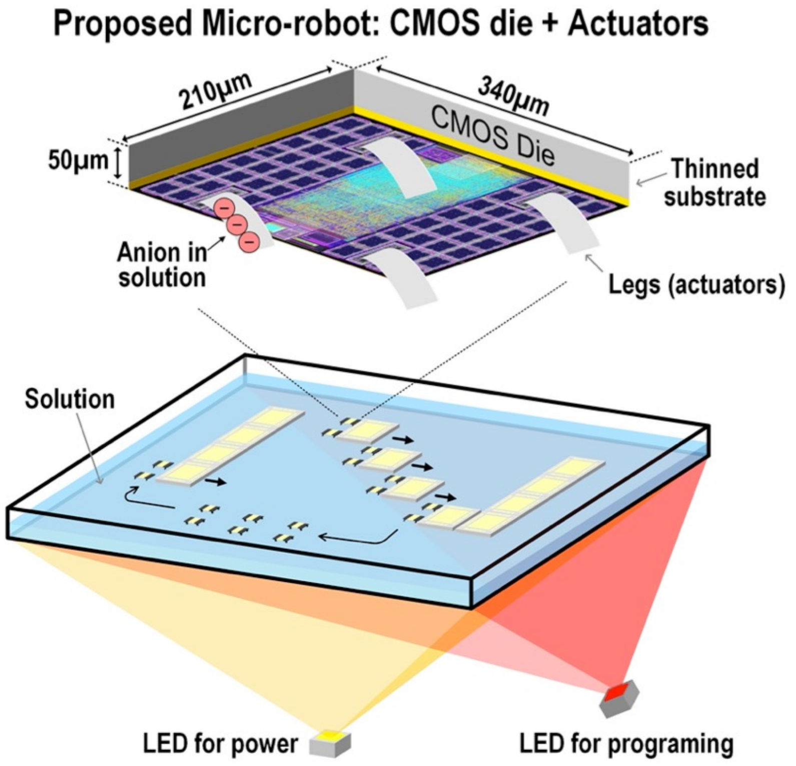
Outline

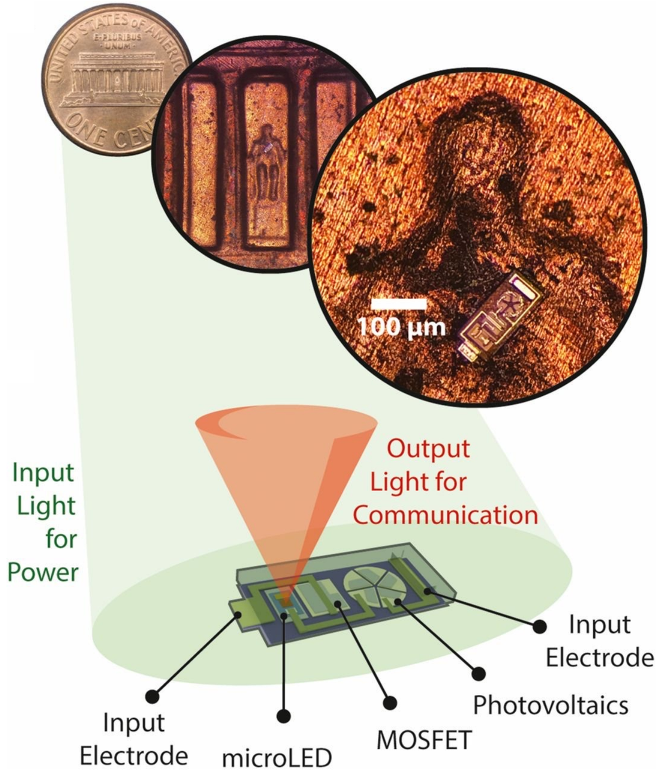
- Motivation & Applications
- Challenges
- THz Energy Harvester Design
  - Optimum Conditions for THz Rectifier
  - Proposed Design of THz Rectifier
- Measurement Results
- Conclusion & Comparison
- Future work: True THz-ID

Applications

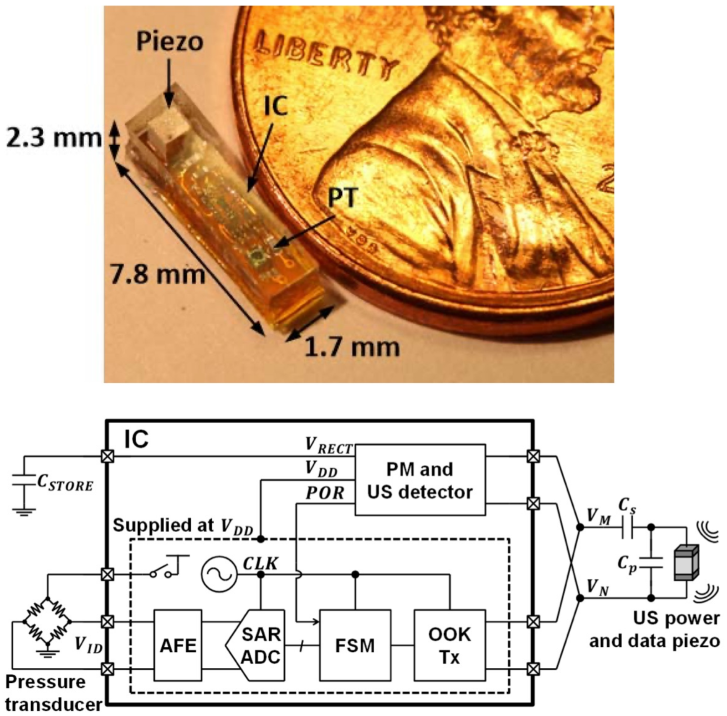
- Ultra-miniaturized platforms are powered by light or ultrasound



Micro-robots
[L. Xu, et al., *ISSCC* 2022]

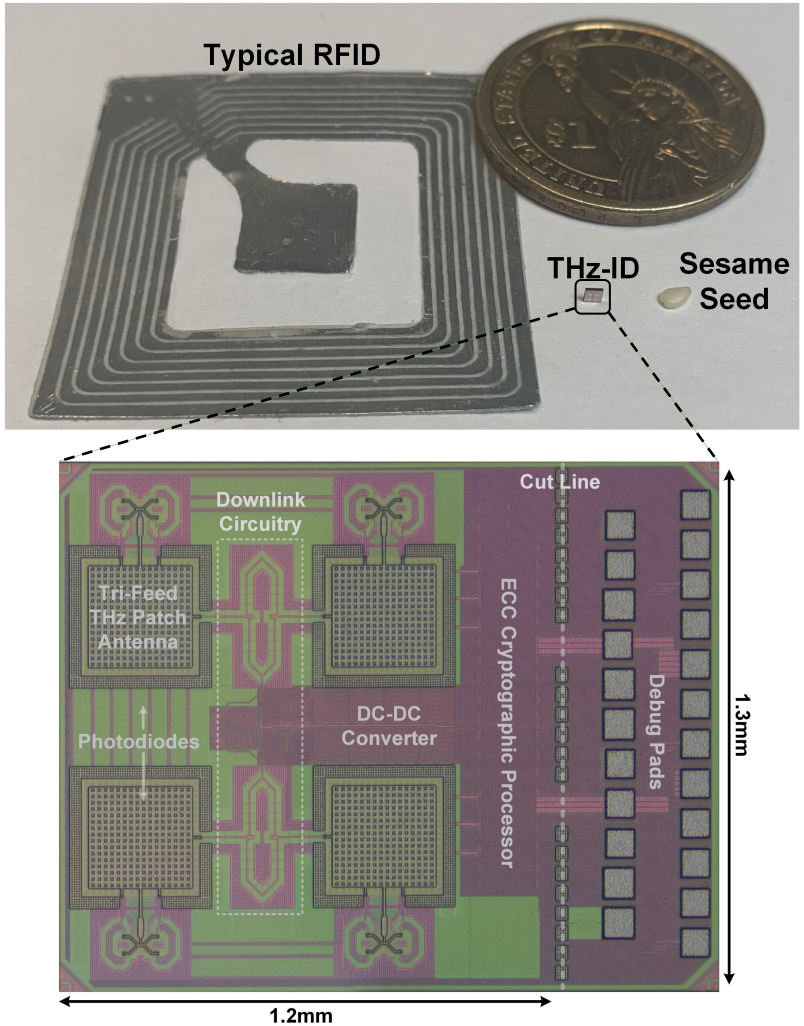


Microscopic Sensors
[J. Alejandro, et al., *PNAS* 2020]

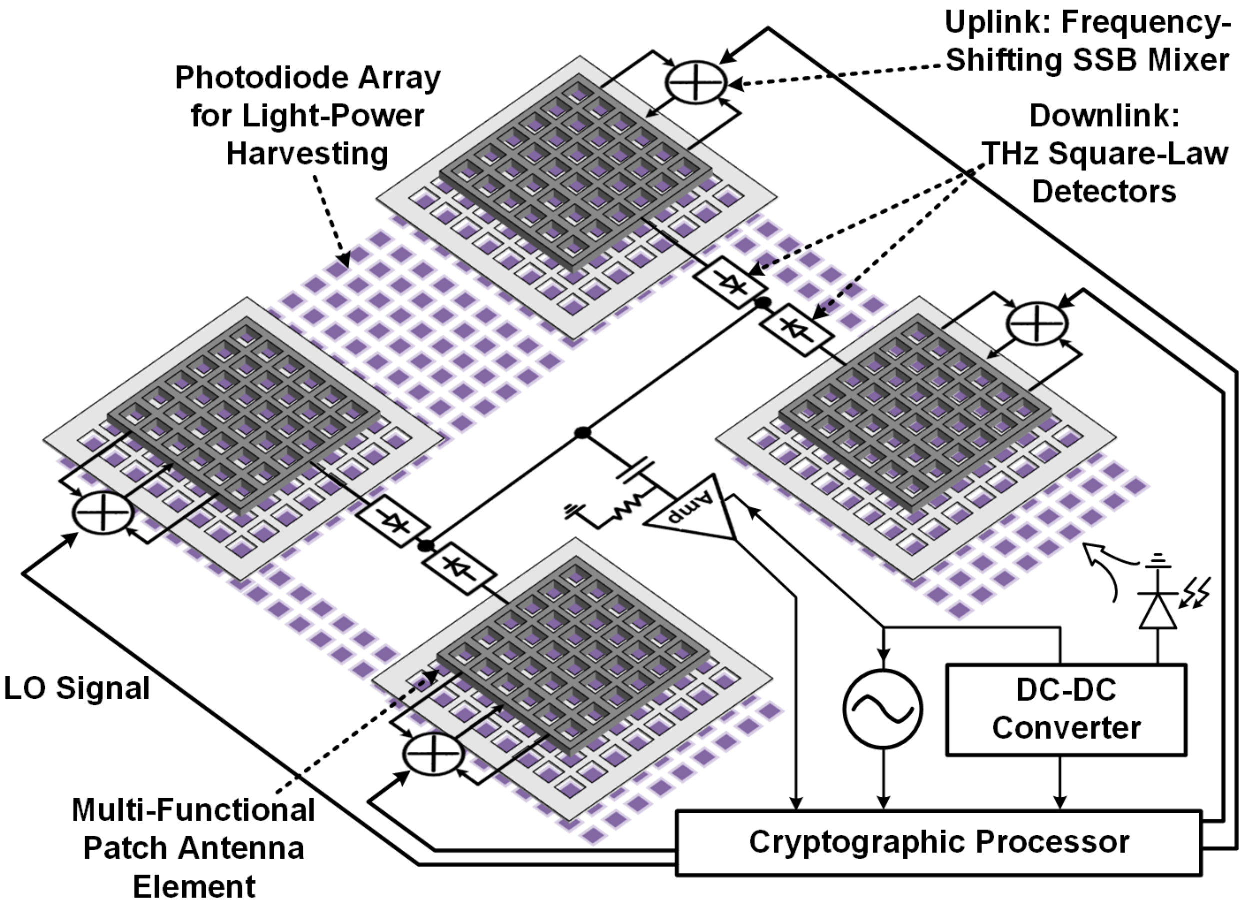


Microscopic Implants
[J. Marcus, et al., *JSSC* 2018]

Applications: THz-ID



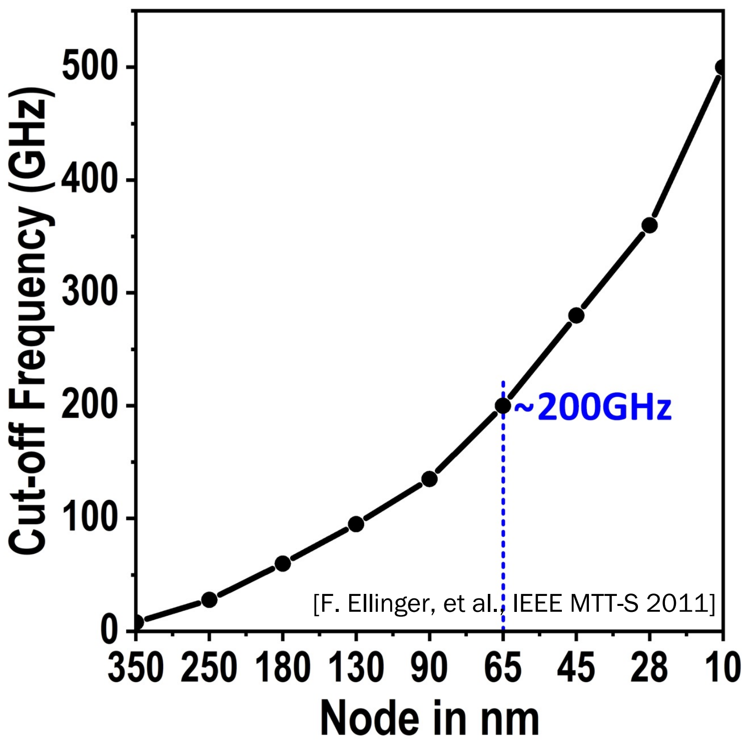
TSMC 65nm CMOS Process



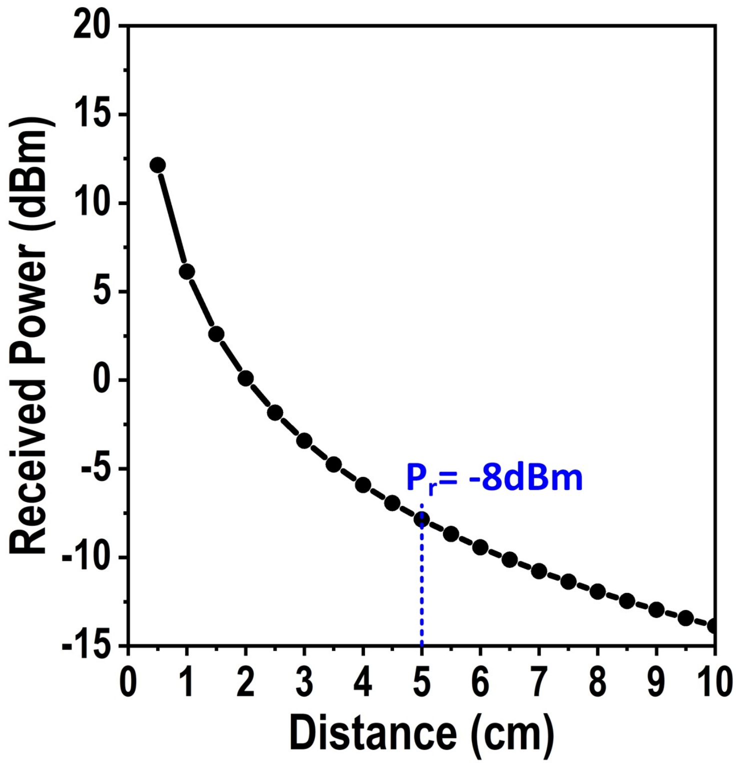
[*ISSCC* 2020, *JSSC* 2020]

THz Energy Harvesting: Challenges

1. Device f_t < 260GHz



2. Lack of high power source



Received Power at 260GHz

(P_t=20dBm, G_t=25dBi, G_r=2dBi)

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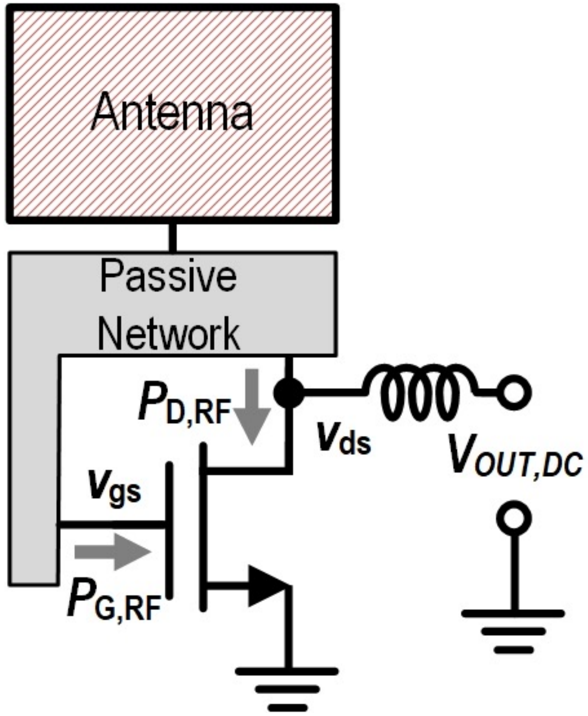
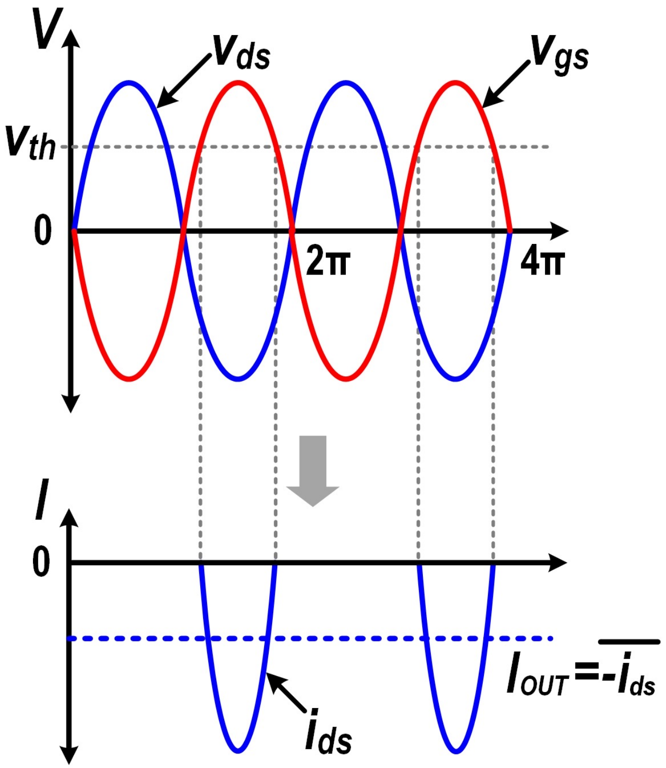
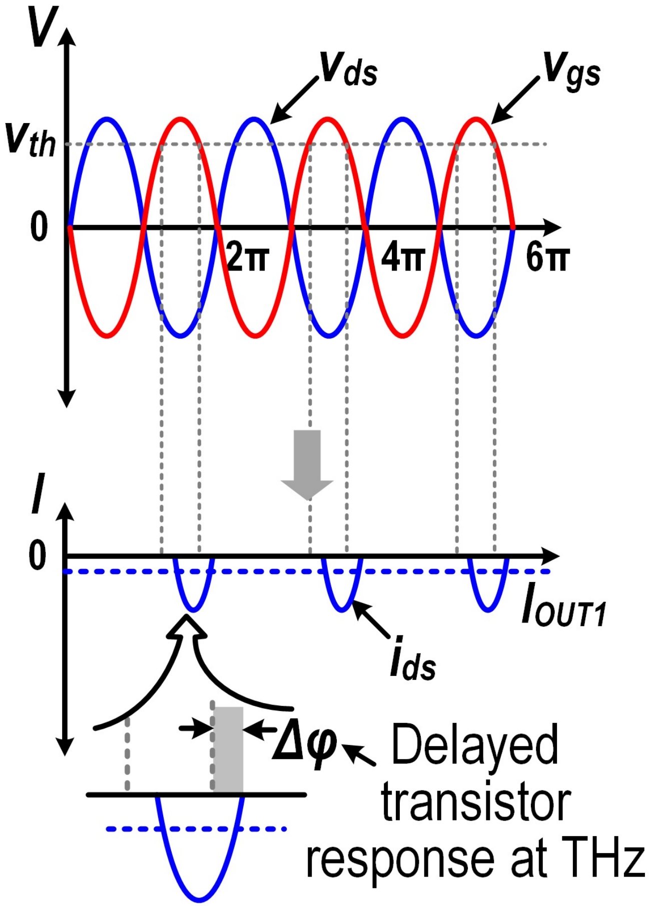
Conventional Switching Rectifier

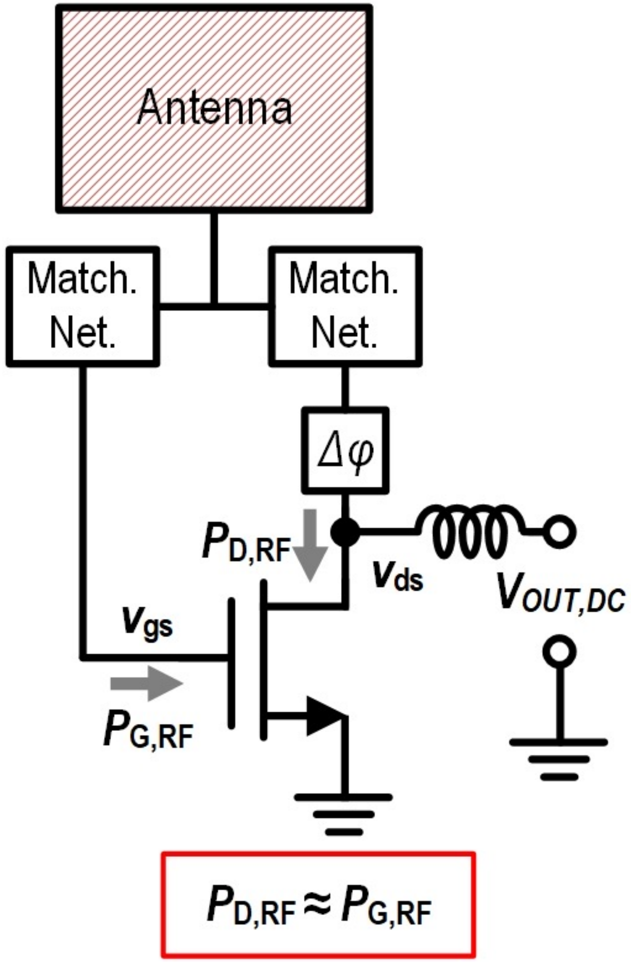




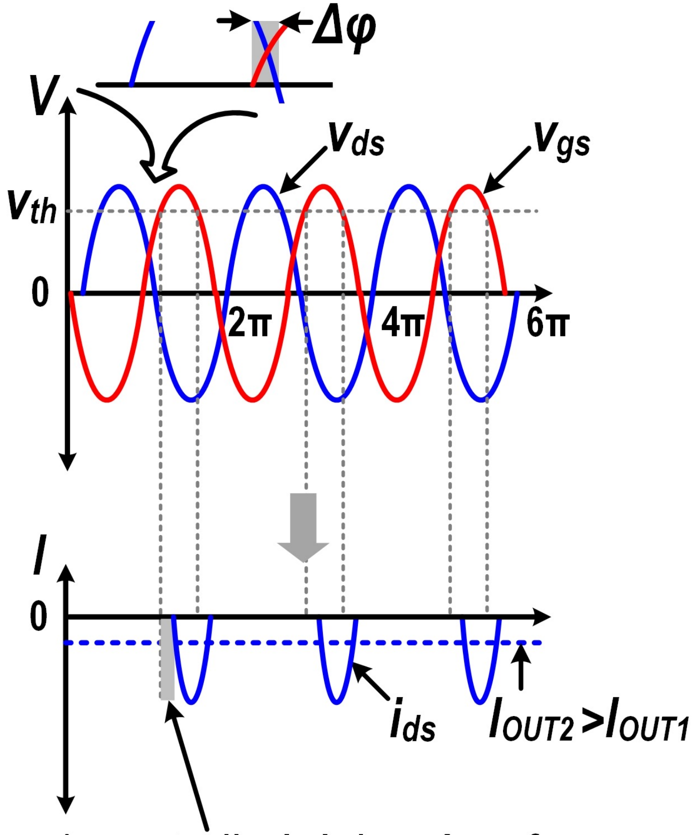
Out-of-phase v_{ds} and v_{gs} leads to optimal i_{ds}



Step-by-Step Optimization

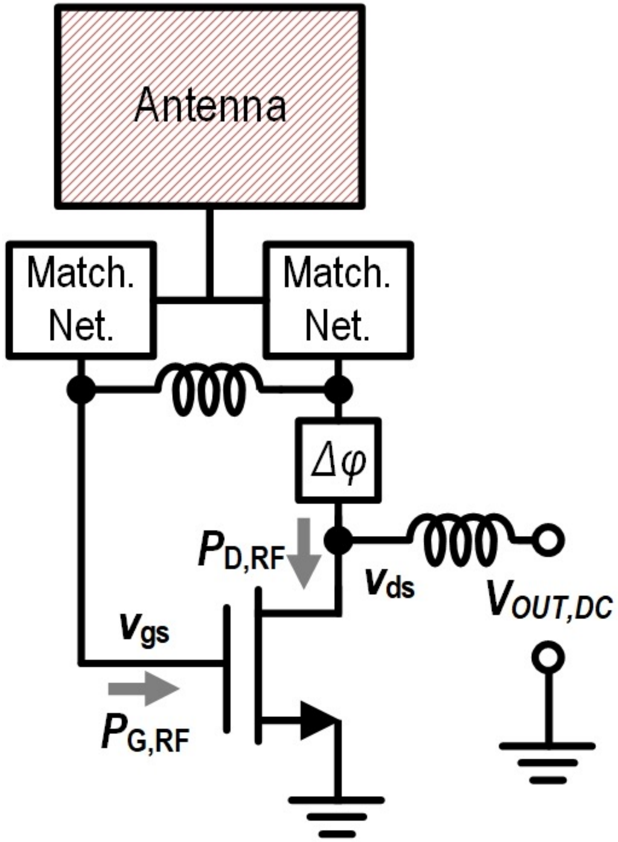


Step 1: Phase Alignment



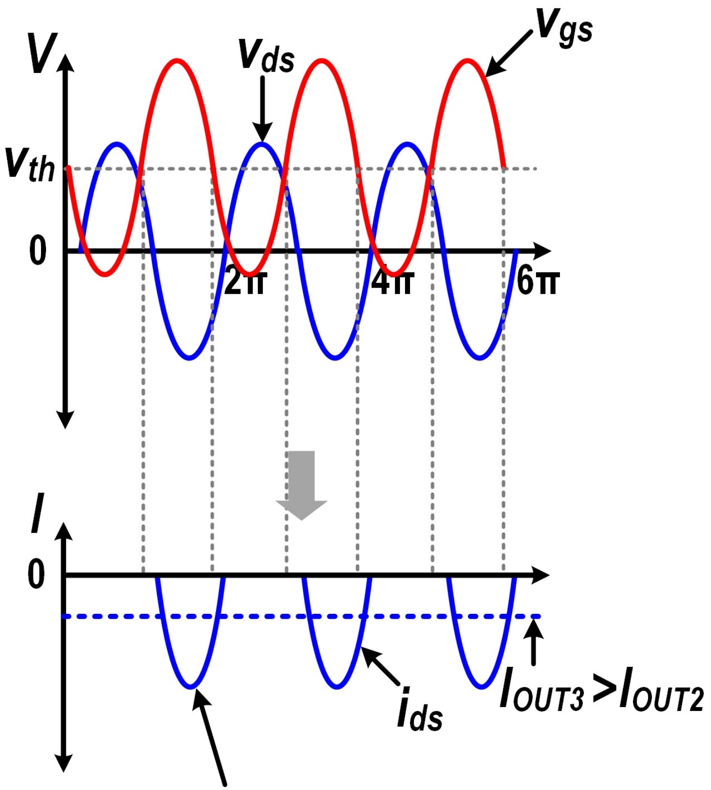
A controlled delay $\Delta\varphi$ of v_{ds} leads to higher i_{ds}

Step-by-Step Optimization



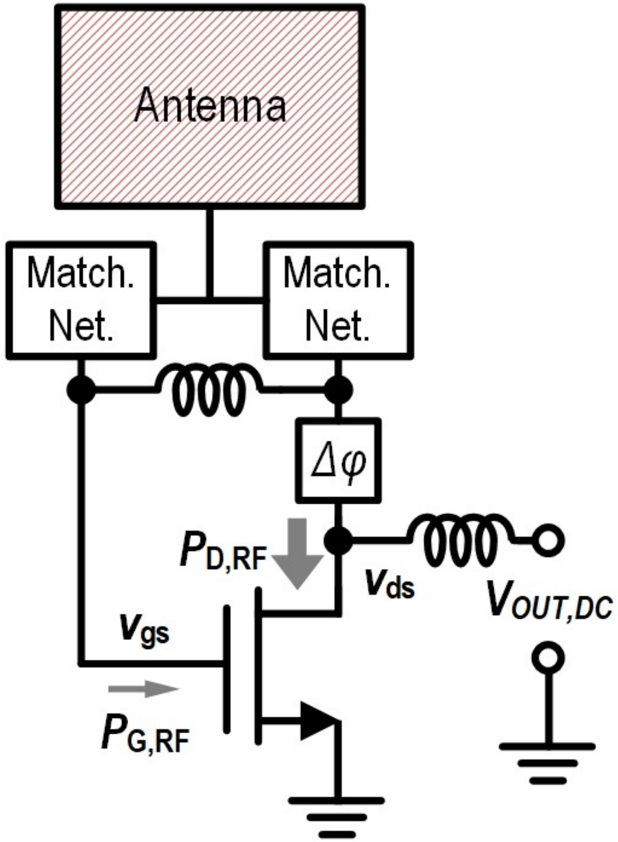
$P_{D,RF} \approx P_{G,RF}$

Step 2: Self-Gate Biasing



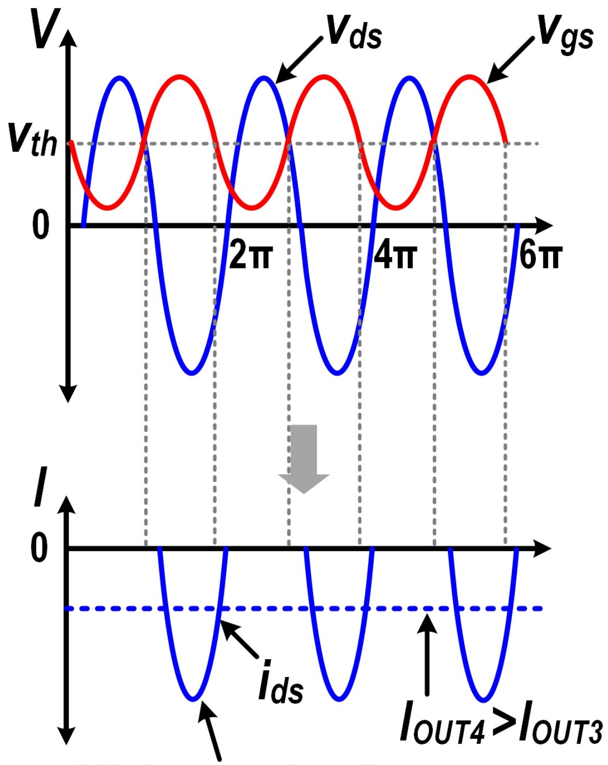
A self-gate bias allows channel to conduct i_{ds} for longer time

Step-by-Step Optimization



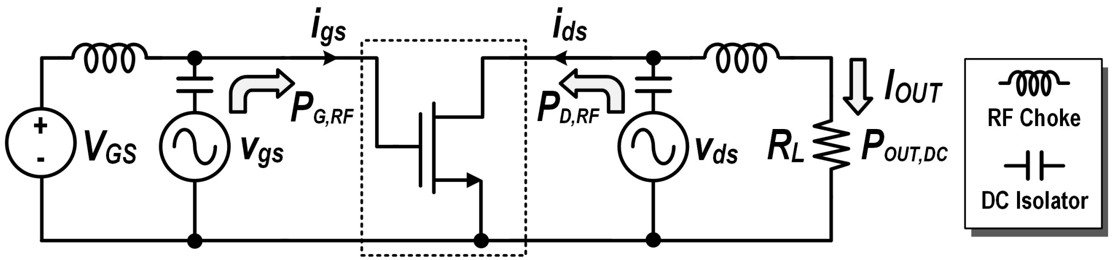
$P_{D,RF} > P_{G,RF}$

Step 3: P_{in} Redistribution

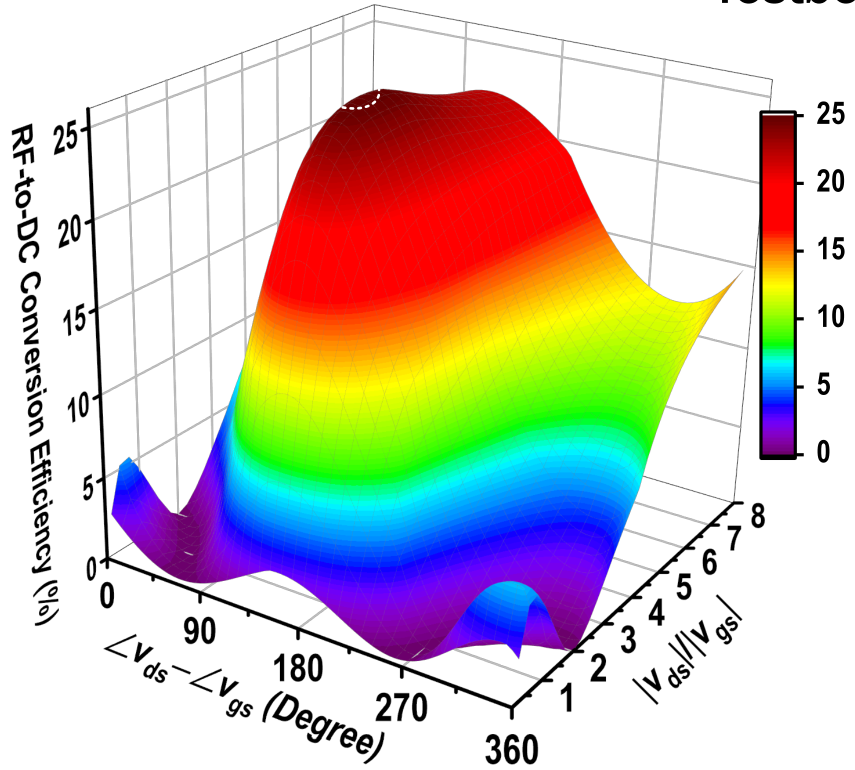


Higher v_{ds} leads to even higher i_{ds}

Simulated Performance



Testbench for rectifier performance



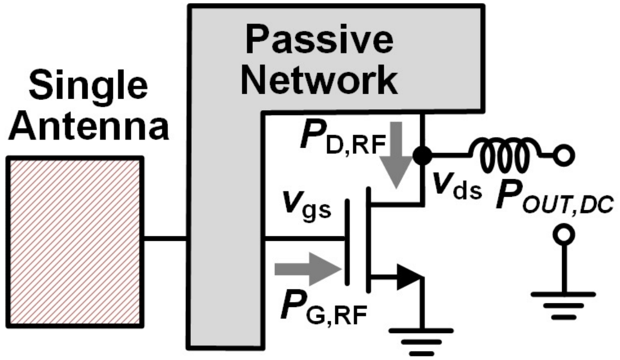
Optimum conditions for η_{max}=25.8% with self-biasing at P_{in}=-8dBm:

$$\Delta\varphi_{opt} = 180° - (\angle v_{ds} - \angle v_{gs}) = 45°$$

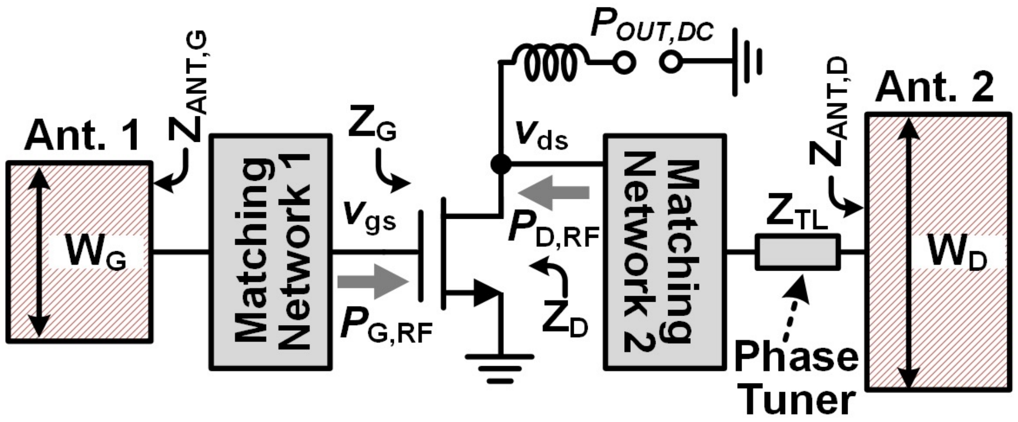
$$A_{opt} = |v_{ds}|/|v_{gs}| = 3.75$$

$$\rightarrow m_{opt} = P_{D,RF}/P_{G,RF} = 2.2$$

THz Energy Harvester Schematic



Conventional Topology



Proposed Topology

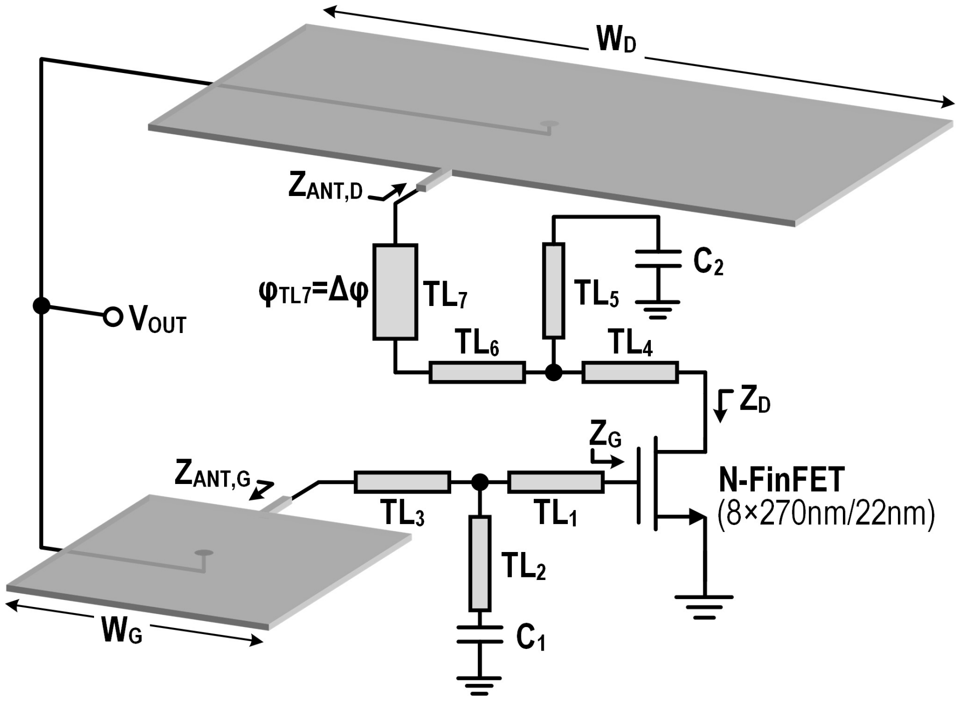
Dual-Antenna Architecture enables

- Separate control for $P_{D,RF}$ and $P_{G,RF}$ through antenna widths
- Independent phase tunning of $\angle v_{ds}$
- Simplified matching networks design

$$Z_{ANT,G} = Z_G^* \quad \text{and} \quad Z_{ANT,D} = Z_D^*$$

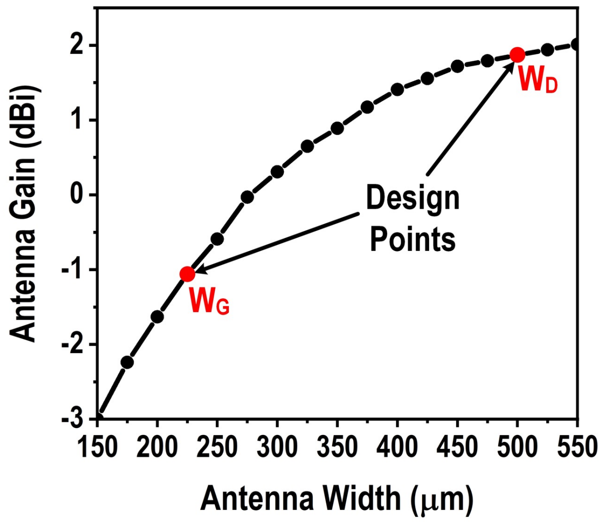
where $Z_G = v_{gs}/i_{gs}$ and $Z_D = v_{ds}/i_{ds}$ are active impedances under optimum conditions

THz Energy Harvester Schematic

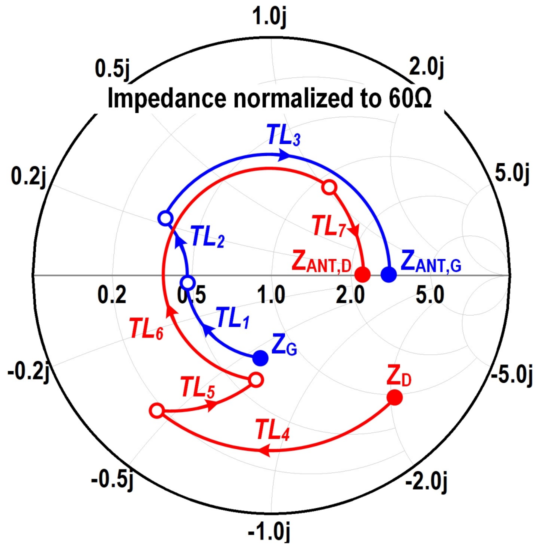


	Length (µm)
TL_1	51
TL_2	73
TL_3	121
TL_4	60
TL_5	93
TL_6	92
TL_7	56

Schematic of 263GHz Harvester

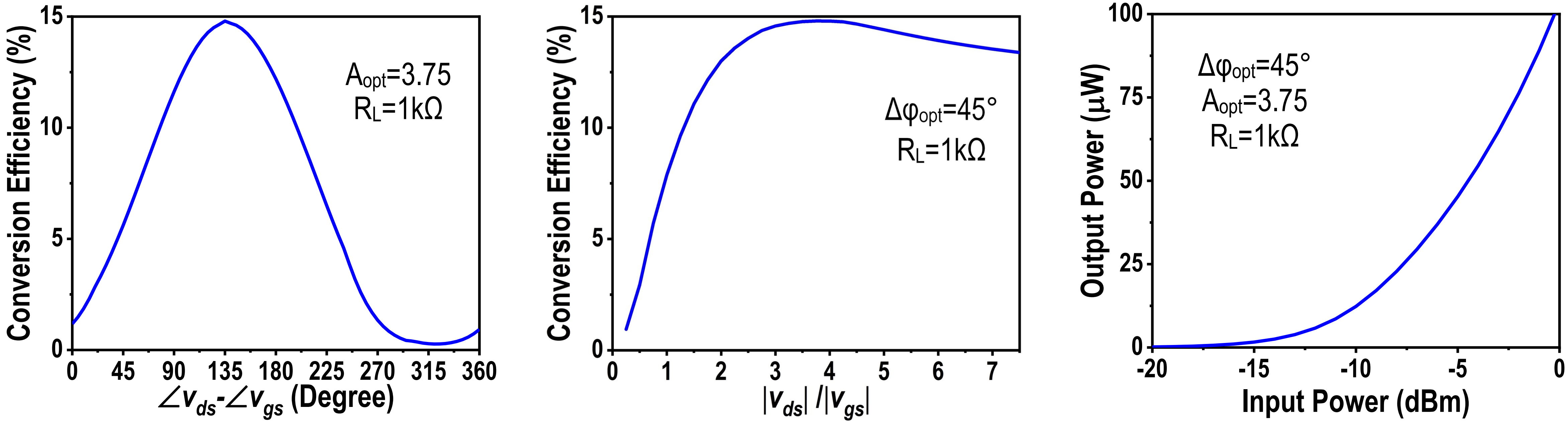


Antenna gain vs antenna width



Gate and drain impedance matching

Simulated Performance



Simulated conversion efficiency and output power including loss of vias and matching networks

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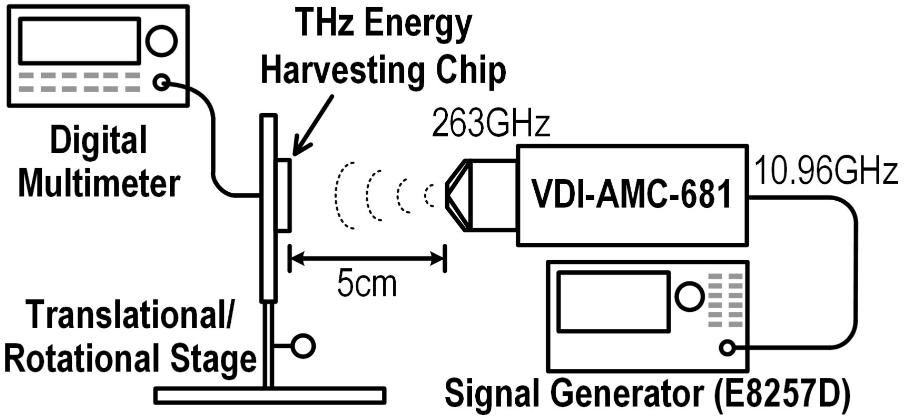
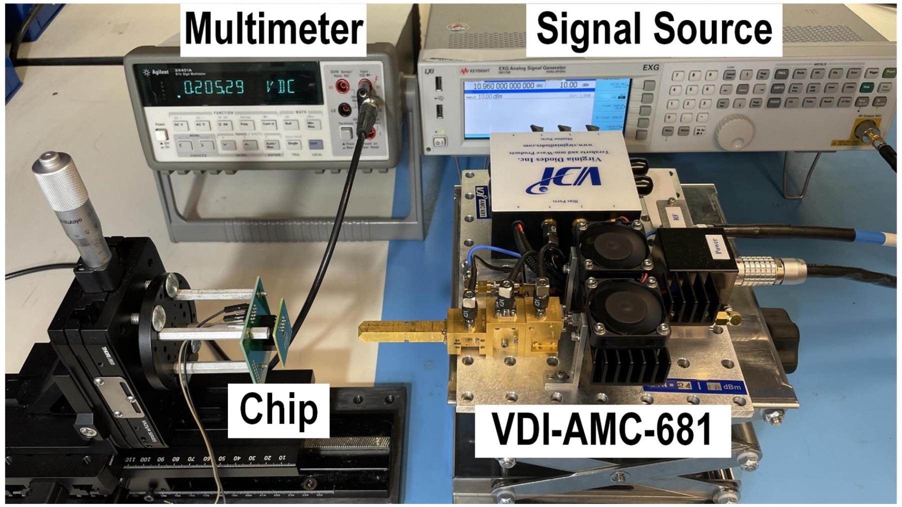
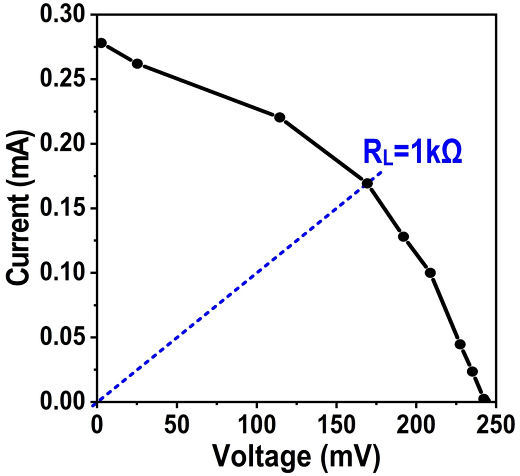
Measured Harvester Performance

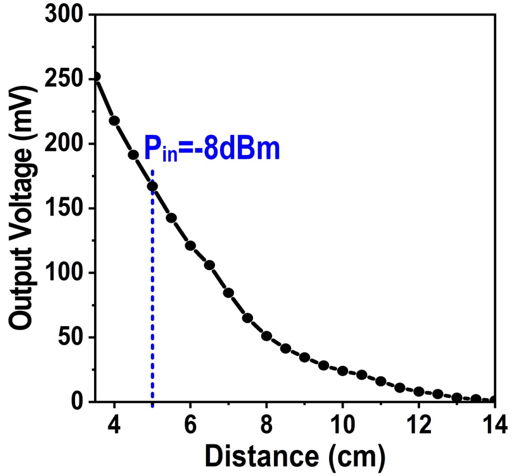




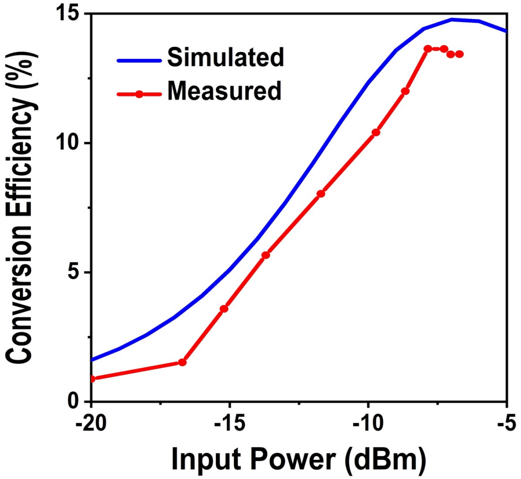
Measurement Setup

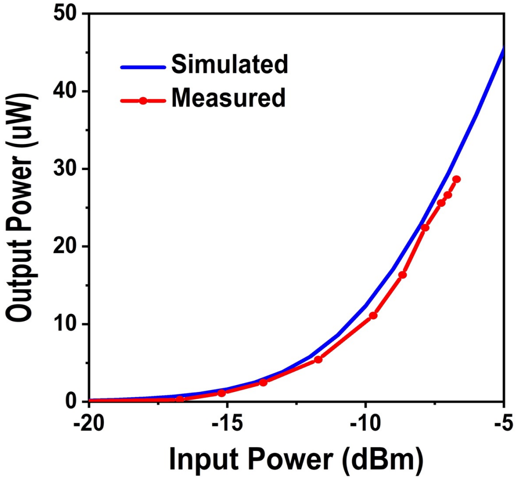


Measured load line



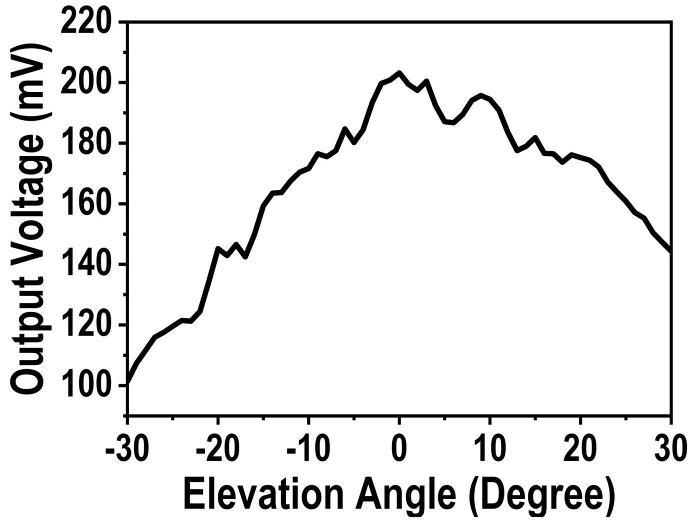
Measured output voltage

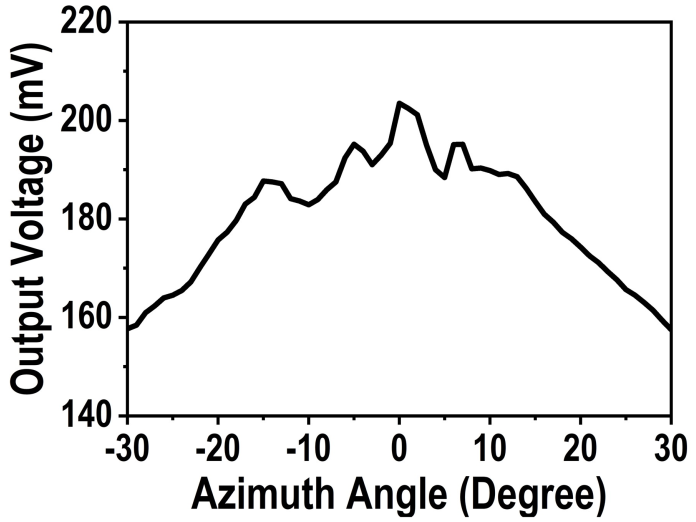




Comparison of simulated and measured η and P_{out}

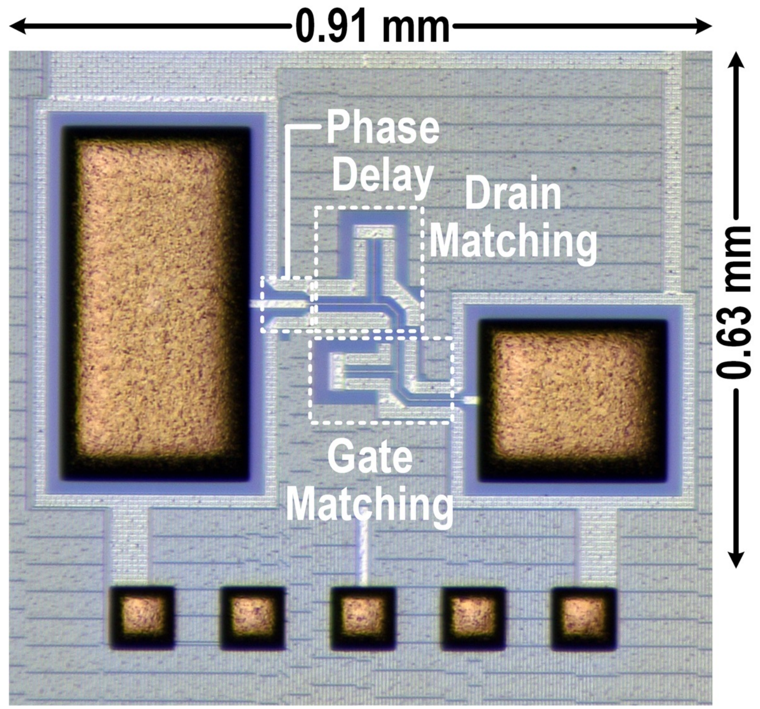
Measured Performance and Chip Micrograph





Measured angle sensitivity

Intel's 22nm FinFET Process



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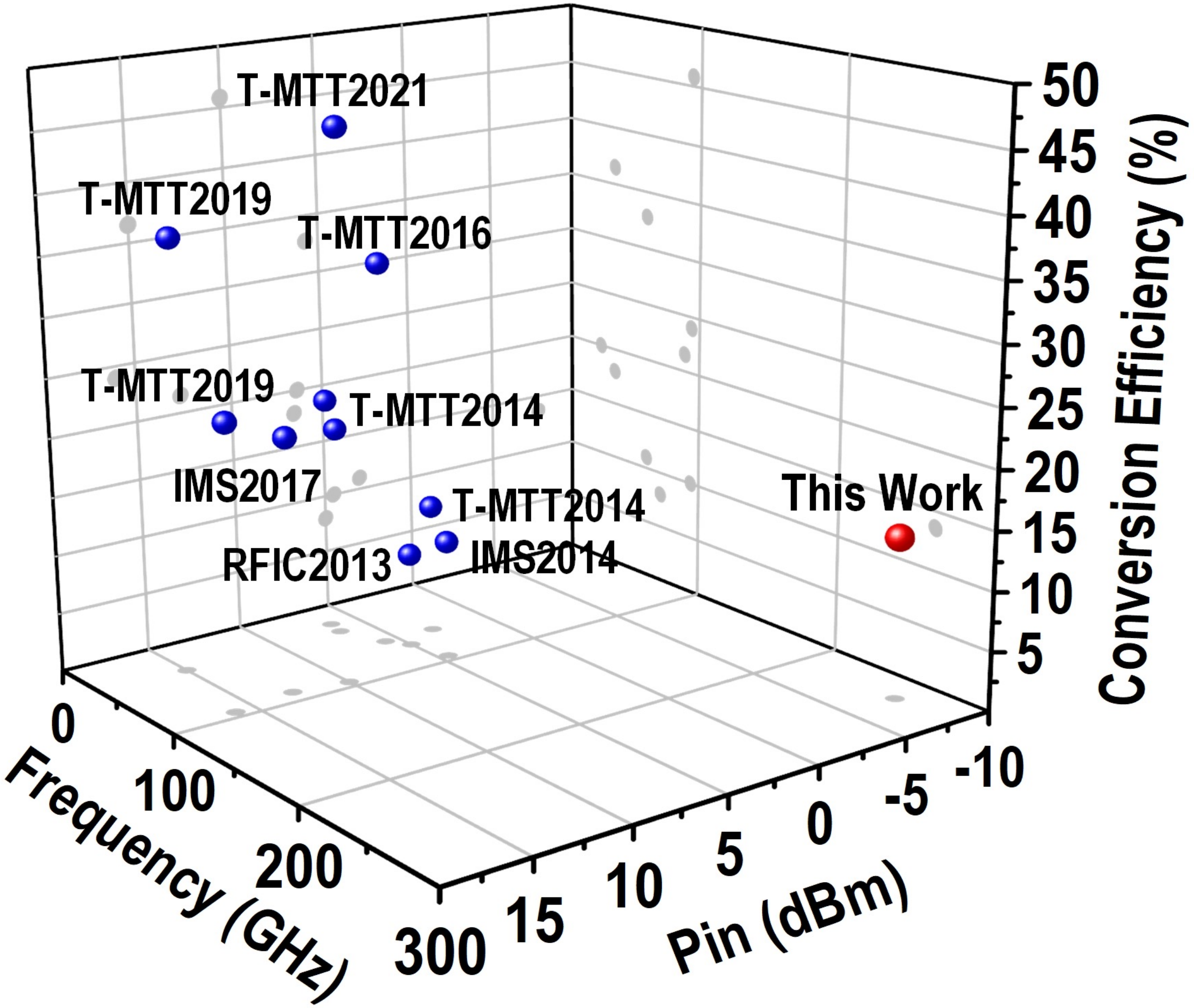
Performance Comparison



Comparison with mm-Wave Energy Harvesters

	CMOS Technology	Frequency (GHz)	Peak Efficiency η_{max} † and Related P_{in}	η at Reduced P_{in} (≤0dBm) †	Area (mm^2)
This work	22nm FinFET	263	13.6% at -8dBm	13.6% at -8dBm	0.57
T-MTT' 21 [1]	40nm Bulk	94	45.8% at 10dBm	5% at 0dBm*	0.08#
T-MTT' 19 [2]	65nm Bulk	94	24% at 16dBm	2% at 0dBm*	0.09#
		35	36.5% at 15dBm	10% at 0dBm*	0.12#
T-MTT' 16 [3]	40nm Bulk	60	32.8% at 5.7dBm	10% at -3dBm*	15600$
T-MTT' 14 [4]	65nm Bulk	24	20% at 6.4dBm	2% at -3dBm*	0.27#
		35	18% at 6.6dBm	4% at 0dBm*	
		60	11% at 3dBm	6% at 0dBm*	
IMS' 17 [5]	65nm Bulk	89	21.5% at 12.7dBm	1% at 0dBm*	0.12#
IMS' 14 [6]	65nm Bulk	94	10% at 4.5dBm	4% at -2.3dBm*	0.48#
RFIC' 13 [7]	65nm Bulk	71	8% at 5dBm	-	1.8#

†Without antenna loss
*Estimated from the plots in the literature
#Area without antenna
$Area including a grid antenna

[1] P. He, et al., *IEEE MTT* 2021.
[2] P. He, et al., *IEEE MTT* 2019.
[3] M. Nariman, et al., *IEEE MTT* 2016.
[4] P. Burasa, et al., *IEEE MTT* 2014.
[5] E. Shaulov, et al., *IEEE IMS* 2017.
[6] N. Weissman, et al., *IEEE IMS* 2014.
[7] H. Gao, et al., *IEEE RFIC* 2013.

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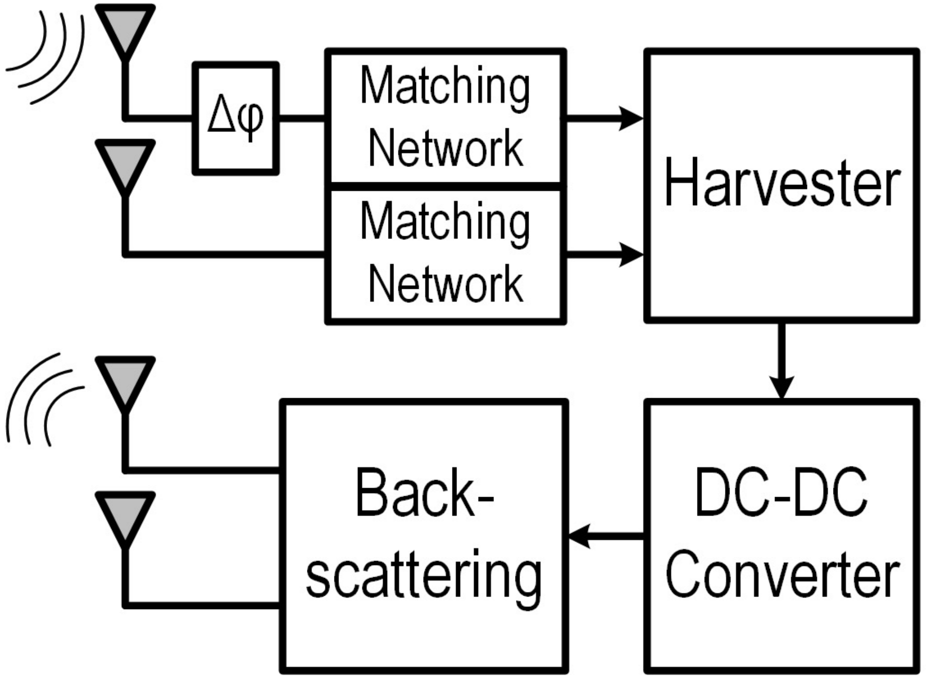
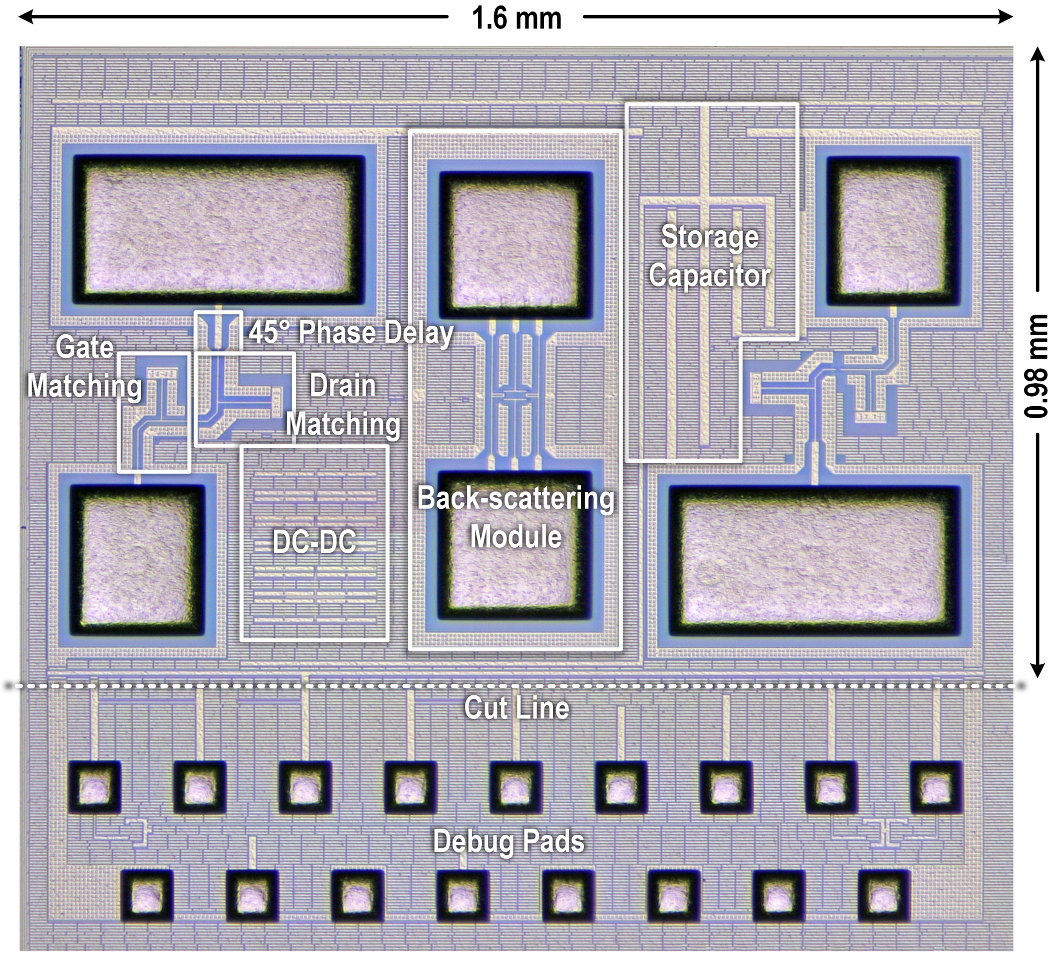
True THz-ID and Chip Micrograph



Schematic of True THz-ID

Intel's 22nm FinFET Process



Acknowledgment

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- I would like to thank Intel's 22FFL university shuttle program for the chip fabrication.

Thank you!