A 265-GHz CMOS Reflectarray With 98×98 Elements for 1°-Wide Beam Forming and High-Angular-Resolution Radar Imaging

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Abstract—The high-angular-resolution imaging capability of future automotive and security sensing systems is in favor of compact, fully integrated, and reconfigurable antenna arrays. The adoption of sub-terahertz (sub-THz) frequencies for such systems relieves the hardware requirements for the physical size and fractional bandwidth (BW). Phased/MIMO arrays, when a large 2-D aperture size is required, are facing great challenges related to high circuit complexities, electronic density, and computation power. This article presents a digitally controlled 265-GHz reflectarray that decouples the designs of active circuits and large passive antenna array. The array is constructed using stitched CMOS chips, fabricated on Intel 16 process, and each unit adopts 1-bit phase quantization and cross-polarization backscatter approaches. With a credit-card size (5.6 × 5.6 cm²), the reflectarray performs 1°-wide pencil beamforming (≈42-dBi directivity) and electric steering within ±60° range in both azimuth and elevation directions. The reflectarray is also equipped with 780-Mb integrated under-antenna memory, which not only eliminates high-speed data communication during raster scan but also enables techniques such as time-dithering sidelobe reduction, and beam squint corrections. Pairing with a commercial sub-THz transceiver (TRX), this work also, for the first time, demonstrates high-angular-resolution, mechanical-movement-free terahertz (THz) imaging.

Index Terms—Angular resolution, CMOS, phase quantization, radar imaging, reconfigurable reflectarray (RRA), terahertz (THz).

I. INTRODUCTION

AUTOMOTIVE and security screening systems [1], [2], [3] have increasing demands for the object-recognition capability of high-angular-resolution 3-D imaging. In most

LiDARs [4] and some high-frequency radars [5], high-angular-resolution imaging is realized through rotational scanning of large, beam-collimating optics; however, the mechanical movement reduces the reliability and portability of the system. A more desired, alternative solution is electrical forming and steering of a narrow beam response based on reconfigurable antenna arrays. Due to the Fourier-like transformation between an antenna aperture area and its directivity [6] (Fig. 1), a sharp beam response (i.e., high directivity), thus high angular resolution, requires a large aperture area (measured by the number of wavelengths) of the antenna array. For example, a 24-GHz radar requires ~60 × 60 cm² aperture area to realize 1° beamwidth (or ~45 dBi directivity), making it impractical to be mounted on vehicles. In comparison, imaging at 265 GHz requires only ~6 × 6 cm² aperture size, which is on par with that of current LiDARs deployed in production cars. Moreover, to achieve 3-D imaging, >10-GHz absolute bandwidth (BW) is required for centimeter- to millimeter-level ranging resolution. To this end, up to 100-GHz FMCW BW has already been reported using a CMOS sub-terahertz (sub-THz) radar transceiver (TRX) [7], [8]. Finally, it is noteworthy that LiDARs [9], [10], [11], while providing excellent resolution, cannot operate reliably under degraded visual (e.g., cloudy, rainy) conditions [12], [13], [14] or strong light interference [15]. In comparison, wave transmission even with cloudy, rainy conditions[12], [13], [14] or strong light interference [15].
dusty, and humid conditions has low loss within a few sub-THz transmission windows [16], [17], [18]. For example, the attenuation in the 200–300-GHz window, with 50% humidity, is below 10 dB/km [19].

Recent research in sub-THz phased/MIMO arrays [20], [21], [22], [23] has made significant progress. The capability of parallel signal acquisition and various multiplexing techniques in MIMO radar makes them favorable to nowadays commercial products. Nevertheless, those arrays are facing increasing electronic density problems, because each element needs an individual active feeding circuit and must be well fit into a small $\lambda/2 \times \lambda/2$ ($\lambda$: wavelength) area to avoid large grating lobes. Techniques based on sparse arrays [24] can relieve such “half-wavelength dilemma,” but still become highly challenging when scaling up to a very large 2-D aperture (e.g., $50\lambda \times 50\lambda$ as this work does) and operating at sub-THz frequencies.

Decoupling the implementation of the active feed circuits and the large phase-shifting antenna array is, therefore, an attractive solution for sub-THz imaging systems. The development of reflectarray, transmitarray, and metasurfaces and surface-wave devices in the past 60 years enables the implementations of electromagnetic structures used as the phase-shifting, passive antenna array. Plenty of works have been done in this field [25], [26], [27], [28], [29], [30], but most of them are at microwave or optical frequencies and are based on off-chip platforms (e.g., PCB, nano-materials), causing problems in large-scale implementations, such as power-consuming phase-shifting devices (i.e., p-i-n diodes), massive signal routing, and complex memory/control/IO units. In [31], GaN HEMT switches are used for the phase control of a $32 \times 32$ element, 235-GHz reflectarray. It is based on a hybrid integration with MEMS waveguide antennas, which realizes high reflection efficiency but also adds cost. It also requires external $4 \times 4$ ASIC control modules and suffers from an estimated $\sim 50\%$ GaN switch yield. A recent 300-GHz transmitarray [32] demonstrated tiled CMOS chip implementation along with a demonstration of near-field holographic projection; its small aperture size ($4\lambda \times 4\lambda$), however, is not suitable for pencil-beam-steering imaging applications.

This article presents a 98 $\times$ 98 unit, CMOS-based, reconfigurable reflectarray (RRA) at 265 GHz using Intel-16 FinFET process, which was originally reported in [33]. The array adopts a 1-bit phase quantization scheme [33] for each antenna element, and thus behaves as a digitally controlled array. One key difference between this work and prior reflect/transmitarrays is it adopts an antenna-level, cross-polarization modulation that reduces the impacts from phase-dependent loss variation and from non-modulated wave reflection. It also leverages the large integration capability of CMOS and is equipped with in-unit memories for all the antenna elements, which not only eliminates large data traffic during beam scanning but also enables other beam-shaping operations, such as dithering-based sidelobe reduction and beam-squint corrections. Using a chip-tiling approach similar to that in [32], this work realizes a large aperture size of $5.6 \times 5.6$ cm$^2$, 1° beamwidth, and electrical 2-D beam-steering in both azimuth and elevation in the measurement. Based on this prototype, a 3-D imaging system is built and demonstrates movement-free 3-D imaging. The remaining part of this article is organized as follows. In Section II, the reflectarray design, including its configuration, antennas, circuits, and assembly, is given. Section III then further describes two specific beam-shaping operations enabled by the integrated memories on this reflectarray. The electrical performance metrics of the reflectarray are characterized in Section IV, and multiple types of 3-D radar imaging results, with a few meter distance and $\sim 0.6$-fps frame rate, are provided. The article is concluded in Section V with a comparison to other state-of-the-art THz beamforming devices. Section V also discusses some possible technical paths to improve the performance and reduce the cost of such systems, to be practical for applications such as autonomous vehicles.

II. Design and Assembly Details

A. Reflectarray Configuration

Fig. 2 shows the 98 $\times$ 98 reflectarray configuration of this work. In comparison to the traditional phased/MIMO arrays, the reflectarray scheme circumvents the aforementioned “half-wavelength dilemma” by only implementing digital control circuits and passive antennas on the aperture. The active sub-THz array feed, which is decoupled from the array design, is not the focus of this work and is hence based on a commercial sub-THz source with custom-designed waveguides to spatially feed the reflectarray. Note that with exactly the same reflectarray configuration, the waveguide feed shown in Fig. 2 can be directly replaced by any on-chip TRXs\(^1\) (TRXs) with any technology, not limited to CMOS. This feature greatly enhances the scalability of the reflectarray and allows for hybrid implementation of technologies (e.g., CMOS reflectarray + III–IV TRX) in one system.

The presented reflectarray is designed at 265 GHz and has a size of 98 $\times$ 98 units with $\lambda/2$ periodicity occupying an area

\(^1\)The TRXs can be either in a monostatic or a bistatic, or even a multi-static scenario, depending on the application of the reflectarray.
of $\sim5.6 \times 5.6$ cm$^2$. For an economical way to realize this aperture with CMOS technology, the reflectarray is divided into $14 \times 14$ abutted chips, each consisting of $7 \times 7$ antenna elements and having an area of $\sim4 \times 4$ mm$^2$. When the incident wave from the feed impinges on the aperture, each antenna element on the reflectarray absorbs the radiation locally and re-radiates it out with a certain phase shift. By properly controlling the phase shifts of all the antenna elements, the reflected wave is reconstructed in a quasi-optical way, and thus generates collimated pencil beams pointing to arbitrary directions in the far-field. Each element also has its own 80-kb memory integrated under the antenna layer and is synchronized by an array-wide clock. These memories, 780 Mb in total, control the phase shifters of each antenna so that the reflectarray performs fully digital 2-D beam-steering.

B. Antenna Element With 1-Bit Phase Quantization

In prior reflectarrays, 1-bit phase quantization [29] has been extensively adopted, because those reflectarrays [26], [34], [35] are mostly based on discrete components and a 1-bit phase shifter significantly simplifies the implementation and control. Using CMOS technologies with dense integration of massive wires/transistors/switches, those advantages diminish, and indeed, mainstream beamforming chips use multi-bit phase shifters for low quantization loss. Nevertheless, in this work, we still adopt a 1-bit phase quantization design (Fig. 3). That is because a multi-bit phase shifter requires a large number of switches in series or in shunt with the signal path. At sub-THz, the inevitable tradeoff between the ON-state resistance and the OFF-state capacitance of these switches causes excessive insertion loss of such multi-bit phase shifters. For example, in the 4-bit, 110–170-GHz shifter in [36], there are eight SiGe HBT switches in series with the signal path and another eight switches in shunt, leading to 20–22 dB of insertion loss. In [37], the 5-bit, 140-GHz shifter uses 36 SOI switches and has 10–12 dB of insertion loss. At higher frequency of 260 GHz, such resolution–efficiency tradeoff further deteriorates. In comparison, 1-bit phase shifter has significantly fewer switches on the signal path, so even when the inherent $\sim3$ dB of quantization loss is included (to be shown next), lower overall insertion loss is expected.

To achieve the 1-bit phase shifting, each antenna element consists of an on-chip patch antenna with two RF switches, as shown in Fig. 3. The antenna is implemented using the top C4 layer (12 $\mu$m thickness) of the Intel 16 CMOS FinFET process, so that the metallic loss of the antenna is minimized and the patch-to-ground distance is maximized. Then the M7 layer is used as the antenna ground plane. The antenna achieves a simulated peak radiation efficiency of 12%. As mentioned in Section II-A, the area below the antenna is filled up with memories.

As shown in Fig. 3, with a linearly polarized incident wave (red) impinging on the antenna, the power is absorbed by the antenna via Port P1, and then reaches a T-junction (gray) through transmission lines. Two identical FinFET switches are implemented on the left and right branches at the T-junction, and their gate controls always have opposite logic voltages. If the right switch is turned on while keeping the left switch off ($D=1$), the sub-THz signal will be further guided to the right branch and re-radiated to free space through Port P2. This results in an equivalent wave reflection, but the reflected wave (blue) has a polarization that is orthogonal to that of the incident wave (i.e., cross polarization). Similarly, if the left switch is turned on while keeping the right switch off ($D=0$), the wave will be re-radiated through Port P3. Therefore, the reflected wave is still in cross-polarization, but due to the geometrical symmetry, it has a 180° phase difference (vector flipping) versus the $D=1$ case. Based on this principle, the antenna shown in Fig. 3 realizes the 1-bit phase shifting for its reflected waves. To facilitate the above re-radiation with cross polarization, the patch antenna has a square shape so that the resonance frequencies associated with the two orthogonal directions are identical.

Here, we make three important notes.

1) Prior 1-bit and multi-bit shifters use different signal path lengths [36], [37] or terminations [27], [31] to control phase, which, however, inevitable leads to different signal amplitudes at varying phases. Our circuit-antenna co-design scheme, on the other hand, only relies on the geometrical reversal and leads to identical amplitudes of the 0° and 180° reflected waves across the entire operation band.

2) In our system illustrated in Fig. 2, the incident wave from waveguide feed is vertically polarized, while the collimated beam after reflection is in horizontal polarization. This feature effectively isolates the wave reflected from the reflectarray from the wave randomly scattered at the structures surrounding the reflectarray, which will be in the co-polarization. It improves the measured
radiation pattern and prevents the random scatters to be injected into the receiver in the imaging setup.

3) To minimize the switch loss in Fig. 3, the FinFET is optimally sized. As shown in Fig. 4, as the transistor size (i.e., number of fins) increases, the insertion loss of the switch in the ON-state drops, but the isolation in its OFF-state becomes worse. Since the actual phase flipping is realized by the differential driving at the P2 and P3 ports, low switch isolation also degrades the overall insertion loss of the switch pair calculated in Fig. 4. Accordingly, the optimal size of FinFET (i.e., eight fins) is determined.

Compared with the normal continuous phase tuning case, 1-bit phase quantization typically causes additional beamforming error manifesting itself as elevated sidelobes. Nevertheless, when pseudo phase randomness is intentionally introduced by the spherical phase front from the array feed, Yang et al. [38] prove empirically that a large-scale array still forms a pencil beam with the same beamwidth as traditional cases, but with a penalty in the array gain. Fig. 5(a) shows the simulated radiation pattern of 1-bit reflectarray with different array sizes (element number \(N\)). It can be seen that once the array size reaches 100 \(\times\) 100, the normalized sidelobe-level (SLL) is well-suppressed below \(-15\) dB. In the meantime, the normalized radiation pattern closely overlaps with the ideal case where there is no phase quantization error, except for the sidelobes far away from the main lobe. The empirical result in [38] shows that 1-bit phase quantization degrades the array gain by 3 dB on average, while 2-bit phase quantization improves the average degradation to 1 dB, and resolution beyond 3 bit provides negligible benefits. With the theoretical calculation in Appendix A, one can plot the curve in Fig. 5(b), which agrees well with the empirical results in [38]. Given the switch loss curve in Fig. 4, it is reasonable to predict that a 2-bit phase shifter needs to double the number of switches, adding at least 2 \(\sim\) 3 dB extra loss, which completely offsets the 2-dB lower quantization loss. In sum, for sub-THz CMOS reflectarrays, the 1-bit phase shifting scheme in Fig. 3 should provide the optimal tradeoff between the quantization and switch losses.

Fig. 6 shows the simulated radiation pattern with 2-D beamsteering, and the 98 \(\times\) 98 element reflectarray is able to provide digitally controlled steering of a 1\(^\circ\)-wide beam in both the azimuth and elevation directions with \(<-15\) dB SLL.

C. Memory Control Circuits

For the 2-D beam raster scanning needed in imaging applications, real-time data communication between the reflectarray and external ASIC(s) or computer for every beam direction change severely degrades the speed and energy efficiency. Instead, it is desired to store the pre-calculated phase-shifter data \(D\) associated with each beam direction on the chips, and then directly load them to the reflectarray antenna during the runtime. Since the Intel 16 SRAM IPs were not instantiated in this design, the under-antenna memory (Fig. 3) is custom-designed with a cyclic architecture illustrated in Fig. 7, which enables repetitive raster scanning of the THz beam. A shift register chain is implemented with two multiplexer (MUX) units on its two ends. By controlling the MUX, these shift registers can be selected to work in a write mode (Mode 1) or a read mode (Mode 2). During the one-time write mode at power-on, the shift registers for all the antennas of a chip are daisy chained, and a sequential data load process...
Fig. 6. Simulated radiation patterns of the 98 × 98 element 1-bit reflectarray. Beam-steering in (a) azimuth and (b) elevation.

Fig. 7. Cyclic memory circuit for controlling the 1-bit reflectarray.

Fig. 8. Die photograph of a single chip and its I/O pad design.

states that are pre-stored for the whole array. After the last stored beam state is reached, the system returns to the first beam state and repeats the steering process.

Although the static power of the digital memory system is low, the massive synchronized flip-flops across the entire reflectarray could still cause large peak dynamic current and voltage supply droop. This is particularly risky since our “chip-stitching” packaging strategy adds nH-level bond-wire inductance in the power supply traces and does not allow external power bypass capacitors for most chips. Three measures are taken to relieve this problem.

1) Small delay gates are inserted along the horizontal CLK signals in Fig. 7, so that the toggles of the flip-flops are spread out.

2) Half of the D-flip-flops of those shift registers are designed to respond at negative clock edge, as explained in Appendix B. This halves the number of clock toggling at the same time, thus halves the peak dynamic current.

3) High-density MIM bypass capacitors are added and distributed across each chip (~90 nF per chip) to establish local power current circulation.

D. Multi-Chip Packaging and Interconnect Design

To facilitate the front-side radiation of the ON-chip patch antennas, the 14 × 14 CMOS chips are attached onto a PCB using a die-attach conductive adhesive material, with their top surface exposed. The micrograph of the CMOS chip and the photograph of the entire reflectarray assembly are given in Figs. 8 and 9, respectively. To circumvent grating lobes, the gap between adjacent chips is kept sufficiently small (<50 µm) during the chip pick-and-place procedure.

To ensure that no significant periodic location perturbation is introduced, the inter-antenna pitch cross the gap (a1 and b2 in Fig. 9) is made to be close (±5 µm) to that within each chip (a2 and b1 in Fig. 9). For the chips not positioned at the array peripheral, the above tight floorplan makes it impossible to create direct bond-wire connections down to the PCB. In our prototype, we adopt a packaging scheme shown in Figs. 9 and 10, where pads from adjacent chips are connected by low-profile bond wires (i.e., chip stitching) and both power supply and data control are fed from the edges of the chip array (through bond wires to PCB) and relayed toward the

2Through-silicon-vias (TSVs) can be an alternative to solve this issue.
array center through the stitched chips. The inter-chip bond wires (wedge bond) in principle introduce extra periodic perturbation. To avoid their interference to the on-chip antennas and to avoid generation of grating lobes, their arch height is kept minimum (about 0.1–0.2 mm based on the comparison with the C4 patch antenna length of 0.27 mm); the scattering on those bond wires also does not possess controlled phase modulation that leads to any power-concentrating lobe in the far-field.

The I/O pad interface of the chip is designed to meet three major requirements.

1) It transfers broadcast signals (e.g., global clock) through the chip area with active buffers installed to maintain signal integrity across long distance.

2) It supports a chip-select signal so that specific commands for an individual chip can be addressed through broadcast signals.

3) It provides solid power/ground connections to maintain power integrity across the whole reflectarray aperture. To meet these requirements, the I/Os of each chip follow the design shown in Fig. 8, and the signaling of the array follows the design in Fig. 10.

Broadcast signal PROG in Fig. 8 controls the chips to work in either Mode 1 or 2. It is important to note that this prototype assembly has more than 2000 bond wires, so a “test-during-assembly” approach is used for risk mitigation. That is realized through a signal DBG used for debugging the chip connections during the assembly process. When the DBG signal is set as high, the chip will bypass all its original circuits and alternate to a simplified 49-bit (1 bit per antenna per chip) shift register chain. This enables a quick check of chip connections by simply streaming small number of bits to the system during the assembly process. Critical interconnects, such as those for clock-in/out and data-in/out, are realized via two redundant pads on each chip (Fig. 8). The global clock is fed into each row of chips. I/O pads CLKi/CLKo are used to buffer and pass the clock to adjacent chips. The memory write-in data signals are also global and routed into all the chips in a similar fashion. In Mode 1 (write), the input data signal (e.g., clock and data) from an on-PCB MUX is fed to only one selected row of chips in the array, so that the remaining rows of chips will not respond (i.e., row selection). Only one chip of the row, determined by the vertical chip-select signal CSX from another on-PCB MUX, is activated (i.e., column selection), so that all its daisy-chained shift registers get programmed upon each clock toggling edge. Other unselected chips in that row only bypass the data and clock. This process is repeated for each chip until all the chips are programmed. Then, the PROG signal puts the entire array to Mode 2 (read).

III. INTEGRATED-MEMORY-ENABLED BEAM SHAPING

When the imaging scanning takes a scan step of one beamwidth (1°), a total ±50° 2-D field of view (FoV) (or 100 × 100 pixels) only requires 10-kb memory for each antenna. In our reflectarray, each antenna has 80-kb memory. The 8× redundancy enables additional beam-shaping operations for each beam direction (or imaging pixel): SLL reduction and beam squint correction.

A. Time Dithering for SLL Reduction

As discussed in Section II-B, 1-bit phase quantization does not introduce much overall gain penalty for the sub-THz reflectarray, but nonetheless it still increases the SLL at angles far from the main lobe [Fig. 5(a)]. In an actual radar imaging system, such extra SLL increases the responses to large clutters, which may mask the actual echo in the main-lobe direction.

To reduce the effective SLL, a “time dithering” technique [28] can be performed in our reflectarray. Note that in a beamforming system, the desired far-field wave interference only mandates the relative phase differences among the elements. The global phase reference/offset of the array, however, can still be freely chosen. Now consider a conceptual signal flow diagram of the 1-bit reflectarray in Fig. 11. The values of
the quantizer outputs \((D_0, D_1, \ldots)\) are determined by both the ideal phases \((\phi_0, \phi_1, \ldots)\), which are determined by the beam direction \(\theta\) and an arbitrary global offset \(\Delta \phi\). The quantization error \(\psi_{1,0}\), which causes the elevation of SLL, has a nonlinear relationship with \(\Delta \phi\). If we fix \((\phi_0, \phi_1, \ldots)\) while changing \(\Delta \phi\) to different values, the main lobe generated by the reflectarray stays in the same direction, but the 1-bit phase quantization errors change in a pseudorandom fashion, scrambling both the amplitude and phase of the sidelobes. Finally, at the imaging receiver output, the complex output data associated with those \(\Delta \phi\) values are integrated, resulting in constructive addition of the main-lobe response,\(^3\) and destructive addition of the sidelobe response, hence reduced SLL. Fig. 12 shows how the sidelobes are scrambled at varying \(\Delta \phi\) and it can be seen that after 4× time dithering (averaging with four different \(\Delta \phi\) values), the averaged radiation pattern is close to the case without phase quantization.

The quantized data \((D_0, D_1, \ldots)\) corresponding to multiple offsets of \(\Delta \phi\) are pre-stored inside the \(\text{on-chip}\) memories, so a 4× memory size redundancy per antenna is sufficient. Since the data loading occurs locally in each antenna, such time dithering for each beam direction can be carried out rapidly and efficiently during the raster scanning, as is shown in Fig. 13. Finally, we note that this time dithering strategy only enhances the contrast of main lobe and sidelobes. The actual power level and the beamwidth of the main lobe are unchanged.

B. Beam Squint Correction

Another issue common in beamformers is the “beam squint.” Our reflectarray is based on a “phase beamforming,” rather than a “true-time-delay beamforming” [39]. As shown in Fig. 14(b), to form an oblique beam angle, it should have a transverse wave-vector \(k_t\) along the array plane, by introducing a corresponding phase gradient. When the operating frequency changes, the overall wavenumber \(k_0\) in the free space needs to change accordingly, but \(k_t\) does not scale due to the phase beamforming. The new vertical wavenumber \(k_z = (k_0^2 - k_t^2)^{1/2}\)

Note that the phase of the output beam at varying \(\Delta \phi\) changes by the same amount \(\Delta \phi\), but such known changes can be later de-embedded at the imaging, so that the main lobe power is added up after integration.

is thus either too small (lower frequency) or too large (higher frequency) to maintain the original beam direction, which is determined by \(k_z/k_t\). As a result, the beam deviates at different frequencies [Fig. 14(a)]. Although the deviation is typically small, for pencil beam scan system with FMCW modulation like in this work, it is already comparable with the beamwidth (1°), hence causing broadened beam response and image blurring. As the simulation in Fig. 14 shows, a 10-GHz scan leads to as large as \(\sim 2°\) beam deviation. With the remaining 2× memory redundancy, we can pre-calculate and pre-store the required phase values \((D_0, D_1, \ldots)\) for two different frequencies within the radar BW. Then, as shown in Fig. 13, during one chirp of FMCW in a radar operation, those data are sequentially loaded so that the beam squint problem is mitigated.

IV. Measurement Results

Each chip of the reflectarray system is fabricated using Intel 16 _CMOS FinFET technology, with an area of \(4 \times 4 \text{ mm}^2\) (Fig. 8). The static power consumption of the whole system with 14 × 14 chips, which is due to the leakage current of the transistors in the shift registers, is 0.2 W. When the system performs 2-D beam scanning, the total power consumption including both the static and dynamic power is 0.85 W under a clock frequency of 100 kHz\(^4\) (Fig. 15).

A. Two-Dimensional Beam-Steering

The setup shown in Fig. 16 is used to measure the reflectarray radiation patterns in both the azimuth and elevation directions. A VDI WR-3.4 Network Analyzer Extender (in the TX mode) is used to generate TX power at different frequencies around 265 GHz. A 3-D-printed polymer waveguide with aluminum coating (see Fig. 9) is then used to guide and illuminate the TX power onto the reflectarray aperture through its WR-3.4 waveguide opening. A VDI WR-3.4 sub-harmonic mixer is placed 1.6 m away and receives the radiated power from the reflectarray system. A spectrum analyzer is used to measure the output of the receiver. Another optional phase shifter is inserted between the mixer and its LO signal source, so that the setup can provide capability of time dithering measurement, which will be discussed in Section IV-B.

A rotational stage is installed beneath the reflectarray assembly so that the prototype can be rotated in the azimuth direction for the radiation pattern measurement. The whole assembly including the VDI feed source can be rotated by 90° and reinstalled on the rotational stage. That allows for the radiation pattern measurement in the elevation direction. The cross-polarization feature of the reflectarray (Section II-B) has already eliminated most of the random scattering at bond wires, PCB, etc. To further reduce the impact of such scattering in this radiation pattern measurement, a BPSK modulation is implemented on the reflectarray by keep flipping all the element bits between 0 and 1 s, while maintaining the same relative bit pattern. Under the memory scheme shown in Fig. 7, this means

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Fig. 12. Simulated radiation patterns for different global phase offsets $\Delta \phi$ with respect to the pattern after time dithering (a) $\Delta \phi = 0^\circ$, (b) $\Delta \phi = 45^\circ$, (c) $\Delta \phi = 90^\circ$, and (d) $\Delta \phi = 135^\circ$. Lower sidelobe level is observed by averaging out the radiation patterns with different $\Delta \phi$.

Fig. 13. Memory data outputs of one array element for time dithering and beam squint correction under FMCW chirping.

Fig. 14. (a) Simulated beam squint of our reflectarray at 265 GHz (nominal frequency) and (b) principle of the beam squint.

Fig. 15. Measured dc power consumption of the array at varying clock speeds for every pre-calculated bit pattern, another dual pattern with all 0/1 s flipped is pre-stored into the shift register chain as well. During the read mode of reflectarray, the original bit patterns and their dual patterns are read out in turn, so that BPSK modulation is accomplished. With that, only the reflectarray-formed output beam possesses this BPSK information and is shown as two sideband spurs on the receiver spectrum analyzer. By measuring the relative power change in one spur, the impact of the above random scattering is completely filtered out. This greatly enhances the measurement accuracy of the radiation pattern, especially its sidelobe level, which could be 40 dB lower than the main lobe.

No array calibration is performed prior to the beamforming operations. Based on the setup in Fig. 16, the measured radiation patterns of the reflectarray in both the azimuth and
Fig. 17. Measured radiation patterns of the work in (a) azimuth, (b) elevation directions, and (c) $1^\circ$ resolution beam-steering.

elevation directions are shown in Fig. 17. It can be seen that the prototype can perform beam collimation with a measured 3-dB beamwidth close to $1^\circ$. Such beamwidth corresponds to a radiation directivity of 42 dBi, which satisfies well with the simulation. In Fig. 17, electrical beam-steering is shown in a range of $\pm 60^\circ$; steering toward larger angles is also supported, though the beam has larger beamwidth and lower power due to the reduced aperture projection toward those directions.

Table I shows the estimated components of $\sim 30$-dB measured insertion loss of the reflectarray. The simulated aperture efficiency [29] of this reflectarray is 27% (or a loss of 5.7 dB). Since the simulated 12% antenna radiation efficiency needs to be counted twice for the wave-reflection process, the antenna contributes an overall 18 dB of loss. As illustrated in Fig. 4, the RF switch loss is optimized to be 2.7 dB. Finally, the quantization loss is estimated to be 3 dB, as explained in Section II-B. The presented reflectarray thus has a gain of $42 - 29.4 = 12.6$ dBi.

B. Time Dithering and Beam Squint Correction

Using the same setup in Fig. 16, we also measure the time dithering performance and beam squint correction of the work. Note that for time dithering, the radiation phase of both the main lobe and sidelobes will be modulated by that $\Delta \phi$ as well. Thus, this extra phase modulation needs to be de-embedded before the signals from different $\Delta \phi$ are added at the receiver side. This is why that extra phase shifter at LO path in Fig. 16(a) is needed. As shown in Fig. 18, just by doing a 4× time dithering ($\Delta \phi = 0^\circ$, $45^\circ$, $90^\circ$, and $135^\circ$), the measured radiation pattern (with a main lobe pointing to $-30^\circ$) already shows up to $\sim 10$ dB lower sidelobes. The integrated sidelobe floor from $-20^\circ$ to $80^\circ$ is decreased by 4.6 dB, and the resulting radiation pattern is even comparable with the simulated pattern without phase quantization. Note that in simulation, the integrated sidelobe floor is decreased by 5.8 dB, and the ideal radiation pattern without phase quantization has a $\sim 7$ dB lower integrated sidelobe floor. The slightly worse improvement of time dithering in measurement compared with simulation may be caused by the extra scattering from the PCBs.

Fig. 19 shows the beam squint correction results. It can be seen that before the correction, the beam squint is $\pm 1.5^\circ$ for a $\pm 5$-GHz frequency sweep. With the help of pre-calculated and pre-stored phase patterns at different frequencies, the beam squint problem can be successfully corrected. Note that the lower measured beam power at 260 and 270 GHz is due to the limited BW of the on-chip patch antennas.

C. Three-Dimensional-Radar Imaging Setups and Results

Further using the 2-D beam-steering ability of the reflectarray, 3-D radar imaging demonstrations are performed. Fig. 20 shows the radar system setup. Here, a VDI WR-3.4 sub-harmonic mixer chain (AMC) is used to generate the 265-GHz power, and together with the reflectarray, they project a sharp pencil beam onto the objects in front of the system. The same VDI WR-3.4 sub-harmonic mixer in Fig. 16 is used as
a standalone, broad-FoV receiver to receive the echo signal from the objects. A function generator generates a triangle waveform for FMCW modulation of the signal source, which then drives both the AMC input and the mixer LO through a power divider. The function generator and signal source are synchronized by a global 10-MHz clock, and that clock is fed into a digitizer (NI PXI-5105) for reference. The triangle waveform from the function generator is also fed into the digitizer to synthesize the FMCW chirp rate. All the instruments are connected using GPIB cables for PC control. The IF output of mixer feeds into the digitizer and then sends to the PC for signal processing. The whole system forms a standard bistatic radar with 1° angular resolution. The FMCW BW used here is ~2 GHz and is limited by the modulation depth of the signal source.

It is noteworthy that ideally, the radar system should have a monostatic configuration (i.e., same waveguide feed port for both TX and RX as shown in Fig. 2) rather than our adopted bistatic configuration; the former allows the TX and RX beams to be perfectly aligned with each other [8] and is more robust against clutter due to the additional sharp response in RX. However, the monostatic configuration requires a directional coupler for the two-way signal duplexing. At this high frequency, the commercially available directional coupler has high loss and thus significantly degrades the system performance. Our custom-made feed waveguide would also introduce additional ~6 dB of loss to the RX path, if the monostatic configuration is used. These accumulated losses eventually eliminate the benefit of the extra reflectarray antenna gain for the RX. Although we adopt the bistatic configuration, we believe the monostatic scheme will still be more advantageous when sufficient hardware improvements are made in the future. This will be further discussed in Section V.

Three types of radar imaging demos are presented. Fig. 21(a) shows an angular resolution test by placing two corner reflectors close to each other (~3°) in the azimuth direction. As can be seen from Fig. 21(a), the corner reflectors are successfully detected and resolved in the radar output dot map, which verifies the high angular resolution of the reflectarray. Fig. 21(b) demonstrates the complete 3-D radar imaging. As shown in the 3-D dot map, all the targets (corner reflectors) in the FoV are clearly detected, with correct (x, y, z) positions. In these two demos, the TX power from the VDI AMC output is ~15 dBm (without counting the ~6 dB loss of the custom-made feed waveguide), and 1 ms of integration time is implemented for the RX, which results in a ~0.6-fps frame rate (40 × 40 = 1600 pixels per frame).
increasing the integration time to 15 ms and accumulating data points in the 3-D space for 30 frames, a 3-D human image can be taken by the radar system, as demonstrated in Fig. 22. Different human body features (e.g., head, chest, arm, and waist) can be clearly seen on the 3-D image, and the body surface contour is reconstructed as well. This shows the feasibility of using THz CMOS reflectarray for future standoff screening applications.

V. Conclusion

In this article, the first CMOS reflectarray system is presented, with 1° beamwidth, in-unit memory, 2-D beamsteering, and 3-D radar imaging. Table II shows the comparison table between this work and other state-of-the-art THz beamforming chips. This work achieves the largest scale and generates the highest angular resolution in both the azimuth and elevation directions. Due to the in-unit memory feature, which was not realized in other works, the presented reflectarray is the only one that has beam profile correction, including time dithering and beam squint correction. The prototype presented here is also the first one that demonstrates high-angular-resolution THz radar imaging without relying on mechanical scan.

In the future, the presented reflectarray can pair with a chip-based sub-THz TRX directly placed in front of the array, which eliminates the lossy feed waveguides and other commercial instruments used in our current setup; that is expected to...
provide better performances and more compact configuration. One challenge associated with such an “all-silicon” system is how a shared TX–RX antenna can be used on the TRX feed side, to avoid TX and RX beam misalignment while not introducing interference. In [8], we discussed and addressed this issue by a radar TRX scheme that avoids using a lossy directional coupler. At present, the high insertion loss of the reflectarray is mainly due to the low radiation efficiency of on-chip antennas. We expect that this problem would be addressed using in-package antennas (AiP) for the reflectarray. Although we are not aware of any report on >200-GHz planar antennas fabricated with mainstream organic-substrate chip packaging processes, our previous 200–300-GHz coupler and channelizer prototypes in an organic chip package [40] demonstrated clear performance improvements over their on-chip counterparts. About 80% radiation efficiency is obtained in the simulation of our preliminary 260-GHz AiP designs. That, compared with the current on-chip antenna scheme (η_rad ≈ 12%), is expected to improve the overall reflectarray equivalent antenna gain from 12.6 to 29 dBi. A monostatic configuration with a TRX feed and an AiP reflectarray, compared with the bistatic scheme with a waveguide-opening RX antenna in Fig. 20, is expected to improve the link budget by 29−12.6 = 16.4 dB in the TX path, and 29−5 = 24 dB5 in the RX path. Such ~40-dB link budget improvement should allow, for example, 15× shorter integration time, thus 15× higher imaging frame rate (i.e., ~10 fps), in addition to 25× longer operation distance (i.e., d = 45 m).6 The AiPs can also dramatically shrink the total area of silicon consumption. With all these efforts, a low-profile and low-cost THz imager suitable for automotive applications should become feasible. In wireless communication, such a beamforming system can be applied to extend the range of point-to-point THz communication links and eliminate the need of the cumbersome high-precision alignment. It may also be used as a hub to address distributed THz sensing/tagging nodes with high spatial resolution. For example, in [42], the MIT team recently showed that this reflectarray system is able to locate and activate a custom-designed 260-GHz wake-up receiver.

**APPENDIX A**

**Quantization Loss Analysis**

Our analysis here focuses on the simplest case in which the output beam is formed in the broadside. Due to the spherical wavefront from the feed, both the amplitude and phase of the incident wave received by each array element are highly distributed, as shown in Fig. 23(a). Here, the red vector represents the single phase reference of the broadside radiation. With continuous phase tuning, all the green vectors are rotated to fully align with the red one. Now with 1-bit phase quantization, the green vectors on the left half of the polar graph should be 180° rotated (labeled in blue), and those on the right remain unchanged (0°), as illustrated in Fig. 23(b).

Suppose each green/blue vector in Fig. 23(b) holds an angle α with respect to the red reference, then the amplitude of each vector can be denoted as a non-negative real function A(α). With different physical scenario of the reflectarray (e.g., Δφ and aperture f-number, F/D), A(α), which represents the probability distribution of amplitude tapering among the array, varies significantly with different α.

The quantization loss in the field intensity, η_p, can be derived by comparing the sum of all the green and blue vector lengths (i.e., continuous tuning) versus the sum of their horizontal components (i.e., 1-bit quantization)

$$\eta_p = \frac{\sum_{i=1}^{N} A(\alpha_i) \cos(\alpha_i)}{\sum_{i=1}^{N} A(\alpha_i)}$$

where N denotes the total element number for the array.

With the assumption of large-scale array, the blue/green vectors become densely and evenly distributed in Fig. 23(b), and thus A(α) becomes a quasi-continuous function A(α), which is essentially like the probability distribution function (pdf) in a stochastic process. The discrete summation in (1) then evolves to integrals

$$\eta_p \approx \int_{-\pi/2}^{\pi/2} \frac{A(\alpha) \cos(\alpha) d\alpha}{\int_{-\pi/2}^{\pi/2} A(\alpha) d\alpha}.$$  

Note that the integral limits stop at ±π/2, because any phase error larger than that is corrected by the 1-bit phase shifting. Since the array feed is located in the center, A(α) is an even function, so that (2) further becomes

$$\eta_p \approx \frac{\int_{0}^{\pi/2} A(\alpha) \cos(\alpha) d\alpha}{\int_{0}^{\pi/2} A(\alpha) d\alpha}.$$  

Meanwhile, larger α corresponds to the incident waves close to the array edges, and thus leads to smaller A(α). Therefore, one may use Gaussian approximation for the pdf A(α)

$$\int_{0}^{\pi/2} A(\alpha) d\alpha = A(0) e^{-\frac{\alpha^2}{\sigma^2}}$$

$$\int_{0}^{\pi/2} A(\alpha) d\alpha = A(0) e^{-\frac{\alpha^2}{\sigma^2}}$$

5The 5 dBi used here is the antenna gain of the RX open waveguide used in Fig. 20, using an estimation based on [41].

6Although the signal path loss is proportional to d4, the equivalent RCS within ∆Φ = 1° beamwidth, assuming the same surface reflectivity of the object, increases with d2. For example, in Fig. 22, the illuminated area of the beam in each beam direction is ∼(dΦ)2 = 1 × 1 cm2. At d = 45 m distance, the illuminated area increases to 25 × 25 cm2, which is still much smaller than a human body.
A finished in each antenna, the whole chain stores 2 bits (Mode 1), when the loop of the cyclic memory chain is to the negative clock edges. Right after the writing mode estimation.

Cases, using 3 dB for the 1-bit quantization loss is a decent gradient for each element in Fig.23(b), and the distribution of directions, one has to further includes the corresponding phase.

If the F/D ratio is large for the array, then the amplitude tapering on the array aperture becomes more uniform. This translates to a near-constant $A(\alpha)$. In that case, (5) simply becomes

$$\eta_p \approx \frac{\int_{0}^{\pi/2} \cos(\alpha) \, d\alpha}{\int_{0}^{\pi/2} e^{-\frac{\alpha^2}{2\sigma^2}} \, d\alpha} \approx \frac{2}{\pi}$$

which leads to a quantization loss $Q$ of 3.92 dB. This is the saturated limit of the quantization loss shown in Fig. 5(b).

Finally, it is worth to note that if the beam points to oblique directions, one has to further includes the corresponding phase gradient for each element in Fig. 23(b), and the distribution of $A(\alpha)$ should be modified accordingly. Nonetheless, one should expect similar plot as Fig. 5(b) for those beam angles. In most cases, using 3 dB for the 1-bit quantization loss is a decent estimation.

APPENDIX B

MEMORY CIRCUITS TIMING ANALYSIS

As described in Section II-C, to reduce the dynamic power consumption of the memory circuits, half of the shift registers there are designed to respond at the negative clock edges. This feature, however, poses non-trivial timing constraints for the shift register chain. Here, the design of the timing is explained in detail.

As shown in Fig. 24, suppose there are in total $2N$ registers per antenna, then the first $N$ registers are set to respond at positive clock edges, while the remaining $N$ registers respond to the negative clock edges. Right after the writing mode (Mode 1), when the loop of the cyclic memory chain is finished in each antenna, the whole chain stores $2N$ bits (e.g., $A_0$ to $A_{2N-1}$). Once the read mode (Mode 2) starts, the whole chain will have a two-step bit shifting in every clock cycle. When a positive clock edge comes, the blue registers all the shifts one bit toward the right, while the red registers stay static. This results in a duplicated register output at the interface between the red and blue registers (red bits in Fig. 24). Based on this feature, the chain immediately loses bit $A_0$ when the first clock cycle arrives. Now, when the negative clock edge follows, the red registers shift one bit toward the right while the blue registers maintain their bits. This results in another duplicated register output at the cyclic interface (blue bits in Fig. 24), but now the whole chain successfully shifts one bit toward right without losing any bit except $A_0$. Starting from the second clock cycle, this two-step shifting procedure repeats but without further losing any more bit. Among the $2N$ registers, there are always two registers storing the same bit. These two specific registers alternate between the red/blue interface and the cyclic interface. Therefore, eventually only $A_0$ in the initially stored bits is lost, and this can be easily rectified during the write mode (Mode 1).

Note that based on this operation, $2N$ registers are able to store $2N - 1$, rather than $2N$ bits. This one-bit lost is the penalty for the half negative clock response, which in return reduces half of the peak dynamic current. Moreover, since an antenna always just reads out the specific bit stored at the cyclic interface, this half-negative-clock-response does not affect the synchronization of antennas among the whole array. Finally, Fig. 24 shows that it does not matter whether the positive or negative clock edge arrives first in each clock cycle. Therefore, the clock phase is irrelevant.

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REFERENCES


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